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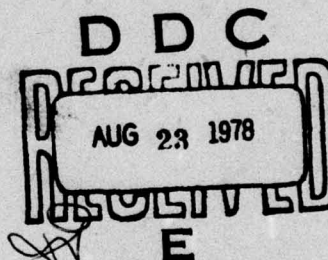
LSI IMPLEMENTATION

J.L. BUIE

TRW Defense and Space Systems
Redondo Beach, California 90278

DECEMBER 1977

TECHNICAL REPORT AFAL-TR-77-261



FINAL REPORT

APRIL 1974 - OCTOBER 1977

Approved for public release: distribution unlimited

Prepared for

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AFB, OHIO 45433

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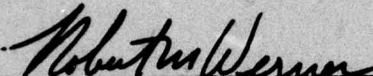
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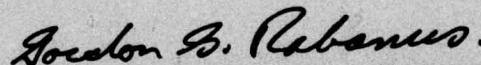
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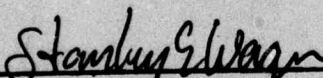


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19 REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM	
1. REPORT NUMBER AFAL TR-77-261	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) LSI IMPLEMENTATION	5. REPORT TYPE & PERIOD COVERED Final Report Apr 1974 - Oct 1977	6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s) J.L. Bute	8. CONTRACT OR GRANT NUMBER(s) F33615-74-C-1103	9. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 6096-01-42	
10. PERFORMING ORGANIZATION NAME AND ADDRESS TRW Defense and Space Systems One Space Park Redondo Beach, California 90278	11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Avionics Laboratory (DHE) Wright-Patterson Air Force Base Dayton, Ohio 45433	12. REPORT DATE Dec 1977	
13. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		14. SECURITY CLASS. (of this report) Unclassified	
15. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		16. DECLASSIFICATION/DOWNGRADING SCHEDULE 12/346p	
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)			
18. SUPPLEMENTARY NOTES			
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Digital Filter, Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Signal Processing Arithmetic Unit (SPAU), Multiplier-Accumulator, Signal Processing Address Control (SPAC), LSI, VLSI, Digital Filter Demonstration Unit (DFDU)			
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This program emphasizes practical hardware objectives in LSI form for implementing digital filters as a general class of applications and the FFT algorithm as a specific application. Three LSI chip designs were completed, the SPAU for signal processing arithmetic unit, the SPDL for signal processing delay line, and the SPAC for signal processing address control. The most comprehensive design, the SPAU, went through two design iterations and the final version has achieved a high degree of acceptance for general filter			

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processing applications. Twenty-five chips each of the SPAU and SPAC designs were delivered. Fifty units of the SPDL were delivered as well as hardware samples of work in progress from time-to-time. Insofar as practical, universal designs were sought and believed achieved, particularly in the SPAU. Based on comparative studies of these implementations and SSI/MSI/LSI alternatives, a large saving in board space, power, and interconnections results from using these generic type LSI chips developed by this program.

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FOREWORD

This work was carried out for the USAF, Air Force Systems Command, Air Force Avionics Laboratory, under Contract F33615-74-C-1103, by TRW Defense and Space Systems, Redondo Beach, California. The technical contracting officer is Robert M. Werner (AFAL/DHE-2).

The work was performed by a dedicated group of individuals at TRW Defense and Space Systems. The Microelectronics Center of TRW had the program responsibility. The program director was J.L. Buie. Considering the scope of the technology involved, help from several other laboratories was essential to completing the tasks. Specific laboratories and individuals contributing to this work are listed below. Thanks are offered to others who also contributed in meaningful ways.

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SECTION I

TECHNICAL DISCUSSION

1.1 Purpose

The purpose of the LSI Implementation program was to design and fabricate LSI Chip types which are practical in reducing the cost of implementing digital filter applications in DOD equipment. Specific objectives are to implement Fourier Transform methods.

1.2 Development Progress Brief

This work started out examining DOD equipment for digital filter applications and centered on digital Fourier Transform methods. It was found that Fourier Transform methods are widely practiced for new designs and considered as a growth application for the general technology trend away from analog to digital equipment.

Various exploratory methods of architecture were under review for the LSI implementation. Of the three general methods for the architecture of the FFT Systems, i.e., serial, parallel-iterative, and array, the parallel-iterative was the only method used on the applications examined. We therefore accepted this as a rallying point for starting this investigation.

Serial methods might be attractive for LSI because of the reduced I/O lead requirements, but on the other hand, very high chip to chip data rates would then have to be used. In keeping within the data rate capability of existing MSI, the new LSI should be compatible since any practical system cannot all be new LSI, but will continue to have reliance on existing supporting hardware. This fact rules out high speed serial methods that would have to be used to supplant parallel processing as now used. The large array processor is at the other extreme of required I/O and represents overkill for the majority of applications. The parallel-iterative approach is the obvious choice for implementing essentially all applications, from parallel-iterative to full parallel array, except the strictly serial processor. Even with the

latter, the introduction of serial to parallel I/O transformation can still retain most of the LSI advantages.

The final result for the principal arithmetic unit LSI went through two major iterations and achieved both a high degree of simplicity and adaptability to general digital filter problems. This is the SPAU 2 which has a parallel multiplier-accumulator organization. Two other chips were also made LSI for implementing the addressing of input data for FFT solution. These were not general purpose but special purpose LSI which were found to have considerable weight on reducing the cost of an FFT system through their MSI replacement factor. These chips were the SPDL for Signal Processing Delay Line, and the SPAC for Signal Processing Address Control. Two designs, the SPAC 1 and SPAC 2 were made for the latter function.

SECTION II

DIGITAL FILTERS

"A digital filter, in broad terms, is any device which accepts a sequence of numbers as its input and operates on them to produce another number sequence as its output."¹ According to this definition, a digital computer or a calculator are the best known examples. However elegant these machines may be, they are perhaps never cost-effective nor capable of real time digital filtering in such applications as communications, radar, and sonar. Such jobs are typically relegated to analog filters or special purpose custom built digital filters. Analog filters are capable of the highest speed performance, but may lack accuracy, versatility, and freedom from drift. It is on these last three factors that any decision to build a digital filter rests.

The fundamental arithmetical operations of digital filters are addition, delay, and shifting. Multiplication, a product of addition, delay, and shifting is further adopted as a convenience. Thus, to build an arithmetic unit, only these four operations are considered necessary to implement in this work. Another consideration is to do each operation in parallel by digital words and increase the operational speed of the electronic machine.

The length of the digital word used in digital filters involves the accuracy requirement and the specific kind of filter used in an application. In general, recursive filters due to accumulation of quantization or round-off errors require greater word length than do non-recursive filters for a given accuracy. The first general purpose Signal Processing Arithmetic Unit design, SPAU 1, uses a 12-bit word length, sign plus 11 bits. This was a compromise since it is difficult to retain sufficient accuracy using 12-bit word length and single precision computation. The SPAU 1, has capability for double precision computation but at the expense of longer programming steps. A second design SPAU 2 also uses 12-bit word length, but all computation on the chip is carried out double precision with much better capability for retaining adequate

accuracy for digital filter problems. The trade-offs between SPAU 1 and SPAU 2 are discussed in detail in the text.

During the period of this contract, 1974 to 1977, the general yield capability of the LSI technology rose from about 5000 devices to over 40,000 devices. The initial design goals in terms of device complexity were set at approximately 15,000 devices. SPAU 1 and SPAU 2 were respectively 15,000 device and 13,000 device LSI Chips. However, the device count was never a limiting factor and much greater complexity could have been used except for practical factors such as package pin limitations. The package pin limit was set at 64 leads and standard flat-packs and dips did not increase over this limit throughout this period. Although timesharing of input/output pins can help and was extensively used in SPAU 1 a penalty is paid due to interference in loading and retrieving information, and efficient programming was more difficult. The SPAU 2 on the other hand has had four ports, two input and two output and the ports are not time-shared. This turned out to be simpler and more generally efficient.

2.1 DIGITAL FILTER STUDY

The end purpose of this work was to implement a wide class of digital filters in LSI and determine the design requirements of such LSI. A joint study was conducted by members of the Systems Group along with Microelectronics personnel. Digital filter systems were taken under review that had previously received design attention using SSI/MSI/LSI devices. These were taken as object lessons for circuit partitioning studies and much was learned with respect to the circuit architecture for a universal arithmetic chip.

The course chosen was further defined as being one where the LSI could be used if it made common sense to do so and not otherwise. It is not expected that cost-effective LSI will be used entirely throughout a system although there may not be technical objections to doing so. For example, RAM memories, ROM's and MSI

buffer electronics will continue to be used. To exclude these fine tuned products for a ritual LSI would overburden the LSI design when it is unnecessary to do so, and detract from the LSI where it should be a worthy replacement.

When is an LSI a worthy replacement? A contemporary digital filter uses MSI/SSI off-the-shelf parts. These are typically general purpose and have considerable flexibility with respect to interconnection by the ample number of input-output leads available. On the other hand, the LSI will be lead limited and have to timeshare leads. It cannot be (the LSI) a one-for-one replacement of disjoint MSI arithmetic if it is to be a worthy replacement. This places an additional burden upon any study, for it most assuredly means that any system will also have to be reconfigured for the LSI and then it can be judged. Such was the method used. Quite naturally a certain a-priori knowledge of what the LSI was to include had to be assumed. The system study then, was a progressive learning experience from one system to the next. The LSI circuit organization was realigned for more effective and universal adaptation as the study progressed.

The first study was on a system called the "K-Band Report Back Demodulator". The FFT Kernel processor portion of this item was configured for LSI and compared with the MSI/SSI version in terms of external interconnect pins, circuit board area, maximum power, and total parts. The LSI design was based on equivalent performance factors with the MSI/SSI actual equipment. The results are shown in Table 1. The savings are approximately 60% in all four categories in favor of the LSI.

A similar study was done using the GPS x User Set (Global Positioning System) as a model. Two electronic processing blocks, the GPS preprocessor block, and the GPS demodulator blocks were redesigned for LSI with approximately the same savings as for the K-Band report back demodulator FFT, 60%.

Another way to look at the LSI and compare it with MSI/SSI savings is illustrated in Figure 1. Here the block diagram of SPAU 1 is reproduced and an estimate of the number of MSI/SSI IC's required to duplicate its function is made.

TABLE 1. K-BAND REPORT BACK DEMODULATOR FFT BUTTERFLY
ARITHMETIC UNIT COMPARISONS

	MSI/SSI K-Band Butterfly	LSI/MSI K-Band Butterfly	LSI Reduction Percentages
Total Maximum External Interconnect Pins	1434 pins	628 pins	56%
Nominal Circuit Board Mounting Area	59 in ²	35 in ²	44%
Total Maximum Power	50 watts	20 watts	60%
Total Parts	76 Dips	26 Dips	66%

As shown in the figure one, SPAU 1 has the equivalent electronic function of 55 TTL IC's. And, based on military grade cost of TTL in the 100 quantity price bracket, the overall equivalent worth of the SPAU 1 is shown to be \$747. The approximate selling price of the LSI tested to military specifications is \$207. Therefore, the direct cost effectiveness of the LSI based on only the packaged chip cost can be several times more effective than the MSI/SSI. If one were to take into account supporting hardware, stocking, incoming inspection, maintenance, spares, additional power supply support, and the like, then the cost effectiveness of the LSI can be even greater.

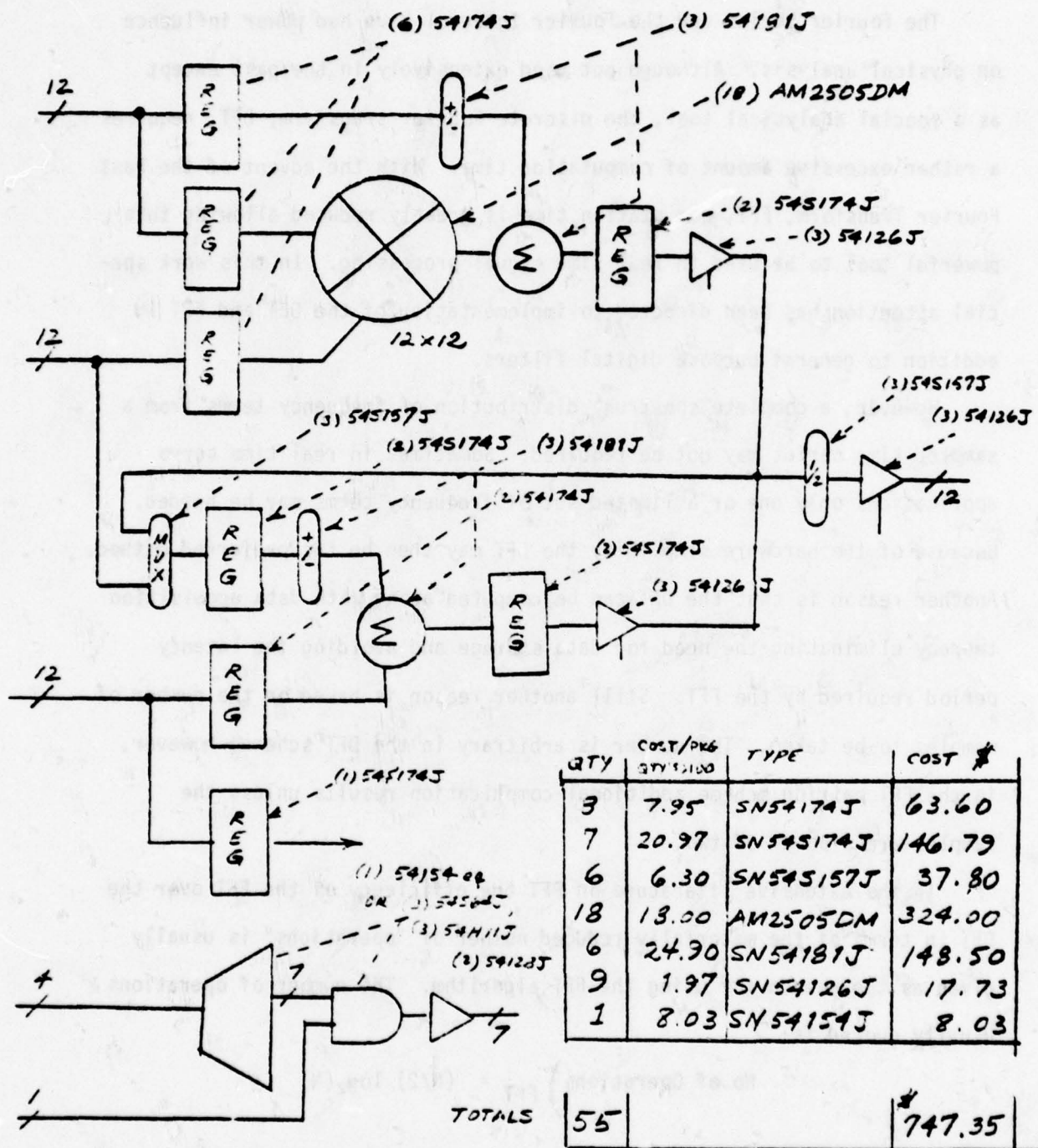


Figure 1. The MSI/SSI Functional Equivalence of the SPAU 1

2.2 Discrete Fourier Transform, DFT

The Fourier Series and the Fourier Integral have had power influence on physical analysis. Although not used extensively in the past except as a special analytical tool, the discrete Fourier transform, DFT, requires a rather excessive amount of computation time. With the advent of the Fast Fourier Transform, FFT, computation time is greatly reduced allowing this powerful tool to be used in real time signal processing. In this work special attention has been directed to implementation of the DFT and FFT in addition to general purpose digital filters.

However, a complete spectral distribution of frequency terms from a sampled time series may not be required. Sometimes in real time servo applications only one or a limited set of frequency terms may be needed. Because of the hardware simplicity the DFT may then be the preferred method. Another reason is that the DFT can be computed along with data acquisition thereby eliminating the need for data storage and avoiding the latency period required by the FFT. Still another reason is based on the number of samples to be taken. The number is arbitrary in the DFT scheme; however, in the FFT pairing scheme additional complication results unless the samples are a power of two.

In the extensive literature on FFT the efficiency of the FFT over the DFT in terms of the materially reduced number of "operations" is usually given as the reason for using the FFT algorithm. The number of operations usually quoted is

$$\text{No. of Operations} \Bigg)_{\text{FFT}} = (N/2) \log_2(N)$$

$$\text{No. of Operations} \Bigg)_{\text{DFT}} = N^2/2$$

where N = no. of data points

Now these expressions in terms of "Operations" depend on how the algorithms are implemented. In this work using SPAU 2 the kernel or butterfly operation for the FFT requires 10 steps of 200 ns each. SPAU 1 utilization is slightly faster, 1920 ns for full butterfly compared to SPAU 2's 2000 ns. The "operation" in the DFT on the other hand is only 2 steps of 200 ns each, each being a multiply and simultaneous accumulation, for 400 ns. Equating these operations performed by the SPAU 2 hardware then has the ratio of DFT to FFT time of solution as follows:

$$\begin{aligned} \tau_{\text{FFT}} &= \left(\frac{N S_{\text{FFT}}}{2} \right) \log_2(N) \\ \tau_{\text{DFT}} &= \frac{S_{\text{DFT}} N^2}{2} \\ \text{Ratio} = \frac{\tau_{\text{DFT}}}{\tau_{\text{FFT}}} &= \frac{\frac{S_{\text{DFT}} N^2}{2}}{\left(\frac{N S_{\text{FFT}}}{2} \right) \log_2(N)} = \left(\frac{S_{\text{DFT}}}{S_{\text{FFT}}} \right) \left(\frac{N}{\log_2(N)} \right) \end{aligned}$$

where: $S_{\text{DFT}} = 2$ Operations at 200 ns each using SPAU 2
(FOR REAL DATA ONLY INPUT)

$S_{\text{FFT}} = 10$ Operations at 200 ns each using SPAU 2

The above formula only considers the case where input data is real for the DFT, otherwise for complex data $S_{\text{DFT}} = \frac{S_{\text{FFT}}}{2}$. Many cases where real sampled data is taken from transducers fits this case. On the other hand, complex input data is almost always required to be computed by the FFT even when the system input is only real data.

Figure 2.2.1 shows a graphical comparison of the ratio of the DFT to FFT solution time. Note that for a small number of points, less than about 32, the DFT is faster for the implied conditions. For a large number of points the FFT method is much faster. However, where a large number of points are collected for solution resolution, but where a full spectrum solution is not

otherwise required, then the breakeven curve shown in Figure 2.2.1 gives the number of DFT output points for equal solution time with the FFT.

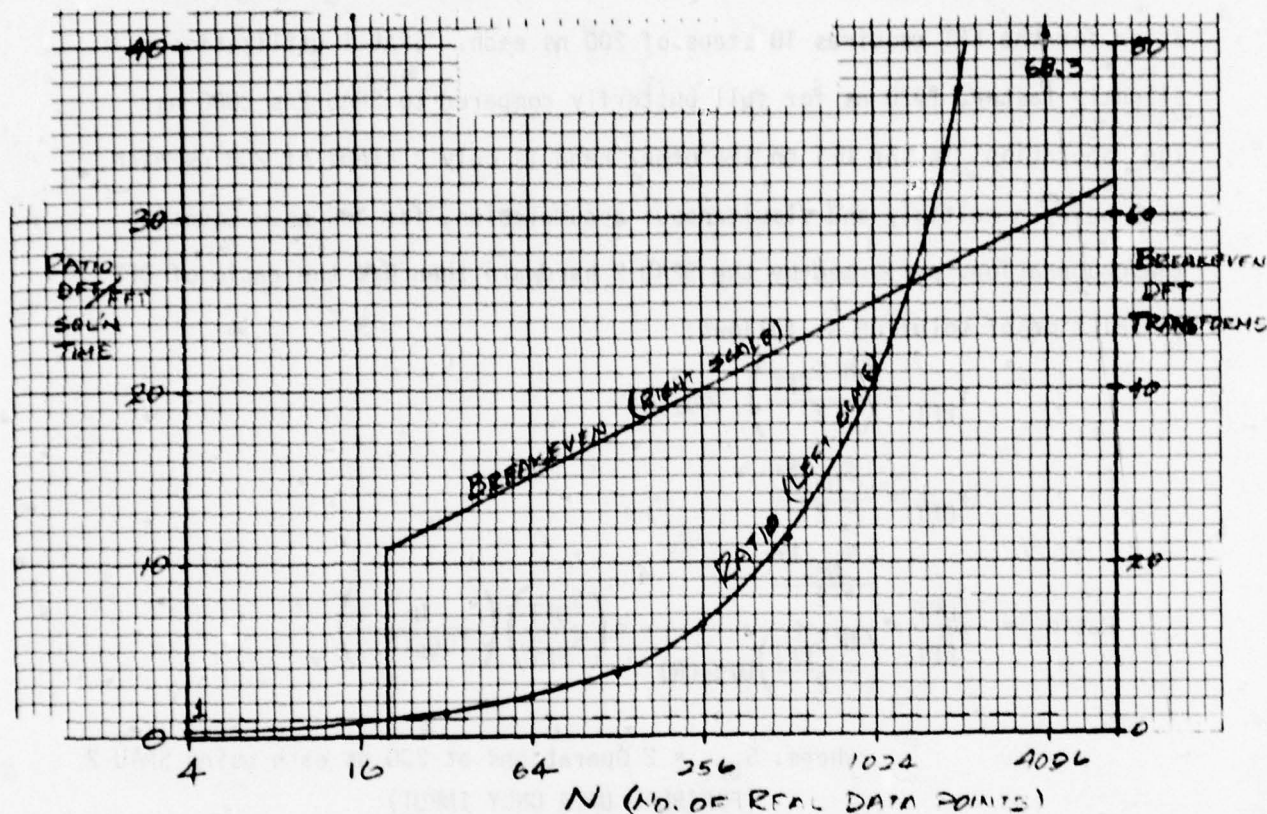


Figure 2. Comparison of DFT-FFT Solution Time

DIRECT DFT, D²FT :

The DFT for time to frequency domain is shown below. Samples are taken uniformly at period T.

$$F_K = \sum_{n=0}^{N-1} f_n w^{nk}, \quad K = 0, 1, 2, \dots, N-1$$

where N = no. of samples

T = Sample period

$F_K = K^{\text{th}}$ frequency term at freq. $\left(\frac{K}{NT}\right)$, $F_K \leq \frac{1}{2T}$

$f_n = n^{\text{th}}$ data sample

$$w^K = e^{-j2\pi K/N} = e^{-je_K}$$

$= \cos \theta_K - j \sin \theta_K$, rotation coefficient

Direct solution for the k^{th} frequency term is then

$$F_K = \sum_{n=0}^{N-1} f_n W^{nk} = f_0 + f_1 (\cos \theta_K - j \sin \theta_K) + f_2 (\cos 2\theta_K - j \sin 2\theta_K) + \dots + f_{N-1} [\cos(N-1)\theta_K - j \sin(N-1)\theta_K]$$

For the case where the samples, f_n , are real and two SPAU 2 are used, one for computing reals and the second for computing imaginaries, the solution time is 200 ns., τ , per step for each frequency component.

This is implemented as shown in the figure below, Figure 3.

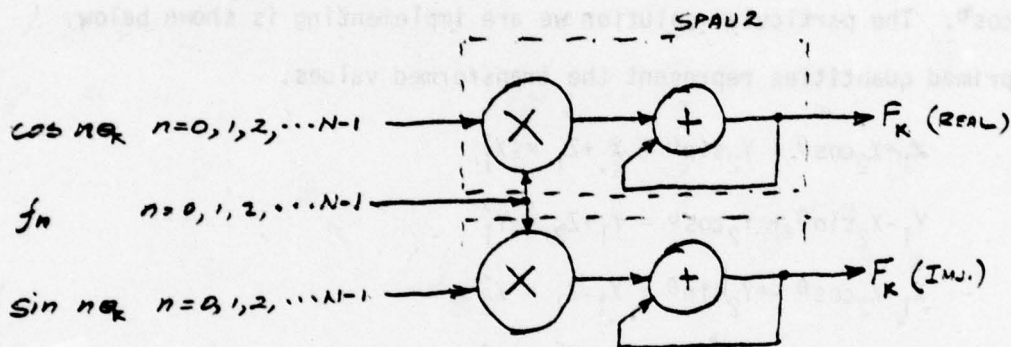


Figure 3. Direct DFT

2.3 Fast Fourier Transform, FFT

As noted in the last section the amount of computation using the D²FT for large N and where the full spectrum is to be analyzed is proportional to N^2 . The FFT methods use a sample index sorting scheme called decimation which results in successively dividing into smaller DFT's. Carried to the ultimate on N samples, where N is a power of two, the array is decomposed to

pairs of samples or intermediate products which connect to other pairs. Each pair forms a computational block. The operation on these pairs by a rotational coefficient is called the kernel operation or more frequently

called a butterfly, from a resemblance of the flow graph diagram to a butterfly.

For solution of the kernel or butterfly we show the diagram in Figure 4. This represents the DFT solution of two points which have been paired by the FFT scheme for time to frequency. The complex FFT points are represented by:

$$\text{1st Sample} \quad X_1 + jY_1$$

$$\text{2nd Sample} \quad X_2 + jY_2$$

These are operated upon by the rotation coefficient functions $\sin \theta$ and $\cos \theta$. The particular solution we are implementing is shown below. The primed quantities represent the transformed values.

$$X_1 + X_2 \cos \theta + Y_2 \sin \theta = X_1' + Z_1 = X_1'$$

$$Y_1 - X_2 \sin \theta + Y_2 \cos \theta = Y_1' + Z_2 = Y_1'$$

$$X_1 - X_2 \cos \theta - Y_2 \sin \theta = X_1 - Z_1 = X_2'$$

$$Y_1 + X_2 \sin \theta - Y_2 \cos \theta = Y_1 - Z_2 = Y_2'$$

Because of the importance of the Fourier Transforms to this implementation work, the DFT and FFT are taken up in more detail in Section 3.

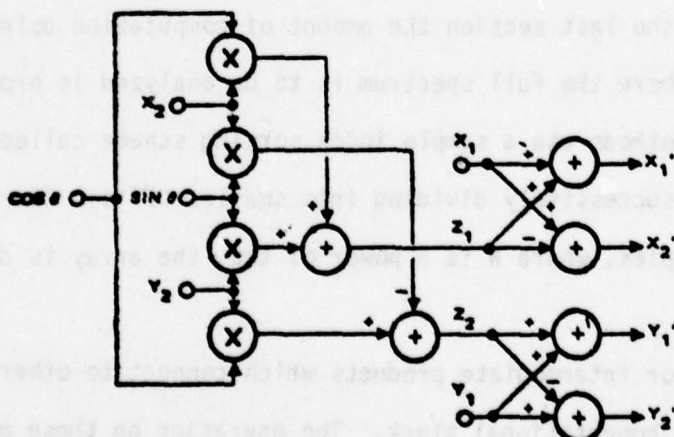


Figure 4. Solution of Butterfly

2.4 LSI Versus MSI Cost Tradeoff

A cost trade-off study was made on a system which we will call a Kernel Processor. This system was a major part of an ongoing design at TRW during the time of the study and represented an MSI application using available TTL MSI MIL grade chips. The LSI designs produced from this contract were taken as the object study, and approximate comparative costs were derived.

The assumptions used in the study are listed below.

- 1) The system life cycle is ten years.
- 2) Parts cost reflected to the customer are 1.43 times actual cost.
- 3) Development costs are 2.63 times actual costs.
- 4) An interest rate of 8% is used to calculate a discount factor of 67% applied to costs distributed throughout the ten year life cycle.
- 5) An attrition, warehousing, and interest costs of 10% per year is applied to all spares.
- 6) A burden factor of 26% is applied to all spares purchases.
- 7) Mounting and wiring costs of parts is 31¢ per pin based on 1-1/2 terminations per pin, including software costs.

The LSI Chip Development costs are taken up first. There is no comparable cost for the MSI trade-off since off-the-shelf MSI chips are used. This item is the greatest penalty the LSI design must overcome for the custom chip design. On the other hand, at the stage when LSI chips of the capability of the SPAU are available, then the development cost would not have to be supported. We take the conservative approach for three new custom designs in this study.

LSI DEVELOPMENT COSTS (3 CHIPS)

1. Partitioning

2. Logic Simulation

3. Timing Analysis

4. Flowcharts

5. Specifications

} System Engineering

(3 Chips) \$95,000

1. Circuit Design

2. Circuit Simulation

3. Layout

4. Verification

5. Fabrication

6. Testing

} Microelectronic Engineering

(3 Chips) \$145,000

Total LSI Development Costs \$240,000

Following the LSI Chip Development, the equipment unit development costs for the LSI and the MSI versions are derived and computed. The material and assembly labor completes the acquisition cost for the first development model built both ways. Costs are listed for both initial and recurring with a one-time 25% learning reduction for the second and subsequent systems. Table 2 shows an itemized listing of these costs.

TABLE 2. KERNEL PROCESSOR

ITEM	LSI \$INITIAL/RECURRING	MSI \$INITIAL/RECURRING
Unit Dev. Costs, 860 hrs @\$15/hr	33,927/0	66,000/0
Integration Labor	4340/3255	5915/4436
Material	6830/5123	8200/6150
Spares	8015/6011	9516/7137
Publication Costs	2000/200	2000/200
Total Initial/Recurring Costs	55,112/14,589	91,631/17,923

Summing up the results it is seen that the recurring LSI costs are 23% less than the MSI version. While not nearly as spectacular as the view taken in section 2.1 (see Figure 1) this is a realistic conservative calculation which takes into account a practical system built using LSI and other available electronics.

If the LSI development costs are to be amortized, then the breakeven number of systems to be built must be 62 units. Thereafter, the savings as listed above would be realized. This calculation has not included weight and power supply savings of the LSI. For air and spacecraft electronics, these could be substantial additional advantages for the LSI.

SECTION III

SIGNAL PROCESSING ARITHMETIC UNIT, SPAU, LSI

The most comprehensive LSI Chip undertaken in this work was the SPAU. The first design of the SPAU 1 was more complicated with more subfunctions and controls than the redesigned SPAU called SPAU 2. Both chips have advantages; however, in terms of simplicity in programming, performance, reduced power, and accuracy in carrying out arithmetic operations the SPAU 2 is superior and represented an evolutionary design step for this kind of hardware.

3.1 SPAU 1, Introduction

Much early attention was given to the SPAU 1 architecture which was derived by examining existing system applications and then partitioning these for efficient LSI usage. The systems examined were ones which used MSI chips and generally performed arithmetic in parallel for high performance. It was our contention that LSI would be proved or not based on its general acceptance as replacement hardware for MSI - not one-for-one replacement, but design concept replaceable for MSI hardware.

The most difficult item to satisfy with the LSI is the limited interconnect compared to the MSI. For parallel arithmetic this generally means timeshared I/O ports and on-chip holding and transfer word wide registers. Also, in keeping with the idea to have this SPAU as flexible and general purpose as possible, the control structure was extensive leading to complication in programming.

The SPAU 1 design was completed and first hardware fabricated. Tests were generally satisfactory except that a few minor problems were found. Two signal inversions and a high temperature V_{CC} sensitivity traced to a saturation condition in the output CML stage was noted. These were readily correctable using minor layout changes and remasking. However, extensive tests carried out on the chip suggested further architecture changes in the control structure by incorporation of a mask programmable PLA. The fixed

microcode in the original design was not optimum and it was envisioned that the mask programmable feature would make the SPAU more attractive for special tasks. The second layout which incorporated these changes was the subject of extensive work although later supplanted by the SPAU 2. In the next section the design aspects of the SPAU 1 are taken in detail.

3.2 SPAU 1, Design

The SPAU 1 has a readily understandable architecture. It does register transfer, parallel multiplication and simultaneous addition, and disjoint addition. It is programmed by means of an on-chip configuration register from off-chip microprogram control or from hardware control. SPAU 1 design handles 12-bit 2's complement parallel words. The simplified block diagram for this chip is shown in Figure 5. Three 12-bit wide inputs are provided. Each has a provision for multiplexing to one of two registers. One 12-bit work output is provided. Registers T, D, and A interface with a 12x12 bit parallel multiplier and simultaneous adder forming the product-sum $D \cdot T \pm A$. Registers P and S interface with a fast parallel adder, forming the sum $S \pm P$. Registers R and X are loaded with respective inputs and interface with an internal transfer bus. The internal bus multiplexes back to register P or to the output tristate off-chip buffers. The sign and 11-bit product, MSB's, are derived from the multiplier-adder. Provision is also available via configuration control to output the sign and the 11-bit LSB product from the multiplier in a second operation back to register A and thence to register R, etc.

The SPAU operations are sequenced and controlled by means of a clock decoder, fast (direct) control logic, and a slow (indirect) configuration register shown as C in the block diagram. Having all direct controls into the chip might further facilitate utilization of the SPAU for diverse applications; however, this would have violated the 64 leads imposed as a maximum for the LSI.

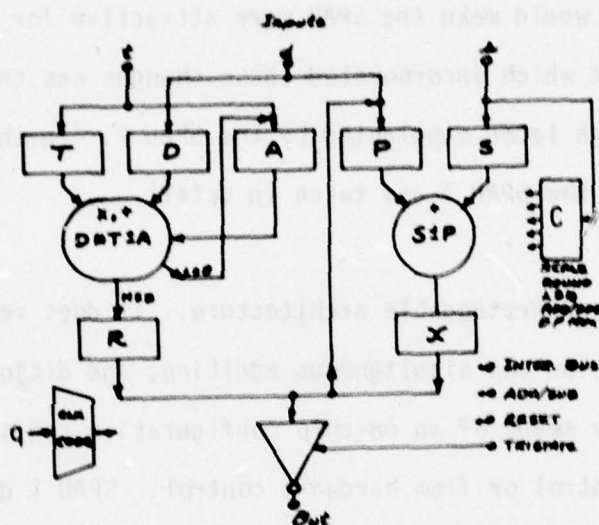


Figure 5. SPAU Block Diagram

A photograph of the SPAU is shown in Figure 6. This chip has 13,800 devices, dissipates 5.1 watts, and has a chip size of 315 x 351 mils. The clock period is 120 nsec, and a typical processing time for an instruction is:

Load D or T and Multiply

	<u>t max</u>	<u>t typ</u>	(nsec)
D register	60	35	
Product driver	25	15	
Product propagation	168	140	
CML R register setup	15	10	
Internal clock skew	10	2	
	278	207	

Time allocated 360 nsec

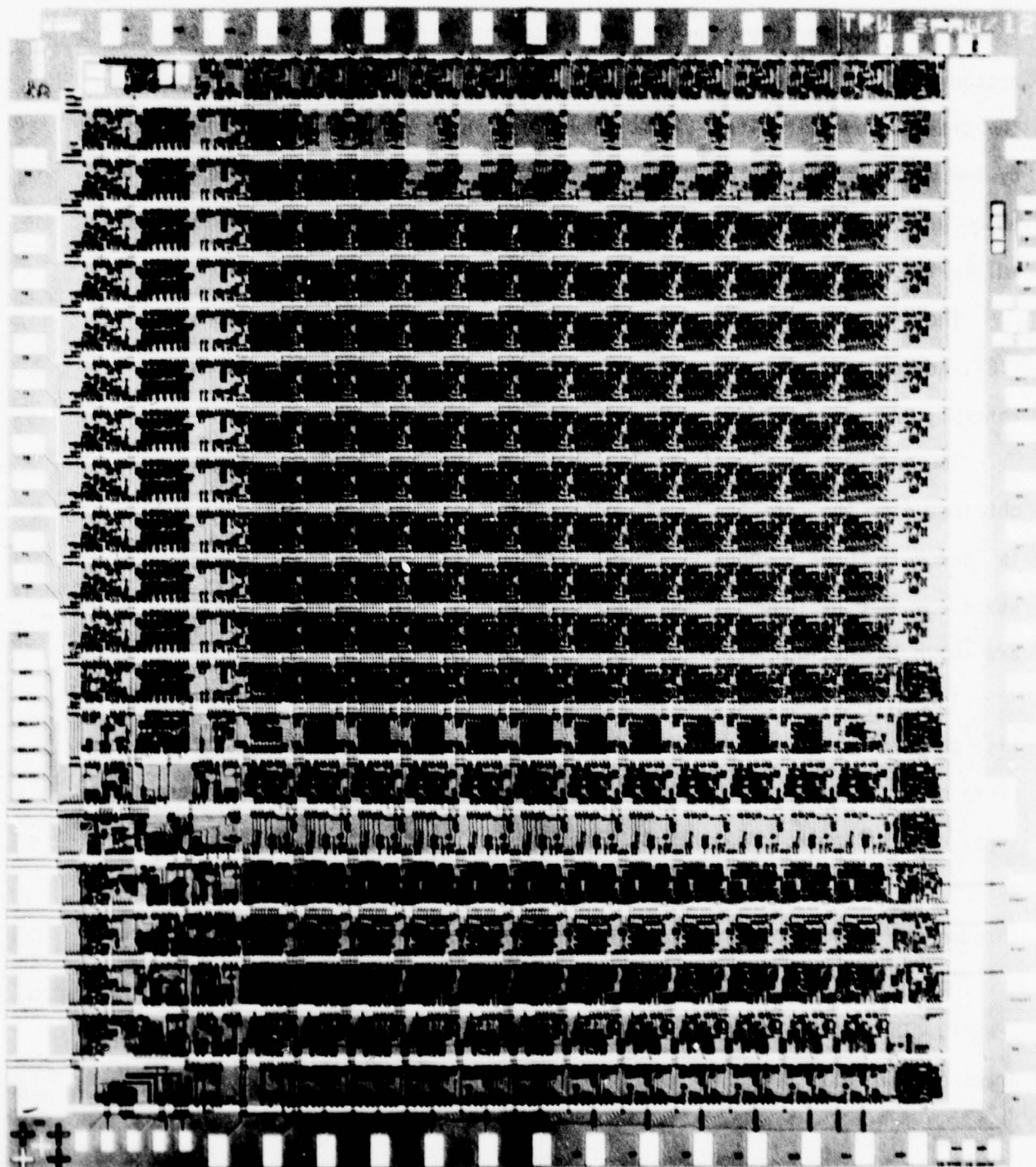


Figure 6. Photo of SPAU

The introductory functional block diagram for the SPAU is again shown in Figure 7. This portrays the control functions by means of switches connected to their respective locations. The input q is a 4-bit input signal to the clock decode circuitry. This determines which registers are to be clocked by the clock input (labeled CLOCK). Input q also has one additional state, KF, which provides multiplexing control to register A for LSB retention from the multiplier.

The direct or fast controls are: Reset, RSTF; internal bus transfer, RTBT; add/subtract for the contents of P register, CADDT; tri-state output control, BZZT; and configuration register clock, C1.

The indirect or slow controls labeled K1 through K5 in the diagram are obtained from the contents of the configuration register C. This, in turn, is loaded from the s input by the C1 direct control. Note that logical "0" state can also be loaded independent of s input. All switches in Figure 7 are shown in the logical "0" state.

The main features of the SPAU 1 are listed in Table 3. Reviewing this list in combination with the functional block diagram is self explanatory. Complete specifications of the SPAU 1 are given in Appendix A. Taking these features and the control flexibility offered, the principal aim of this organization for the SPAU has been made to allow pipelining digital filter algorithms through one or more of these LSI chips depending upon performance requirements.

Appendix B is a detailed layout and circuit design discussion for the SPAU 1. The method of layout, cell placement, signal routing, schematic diagrams of all cells are given.

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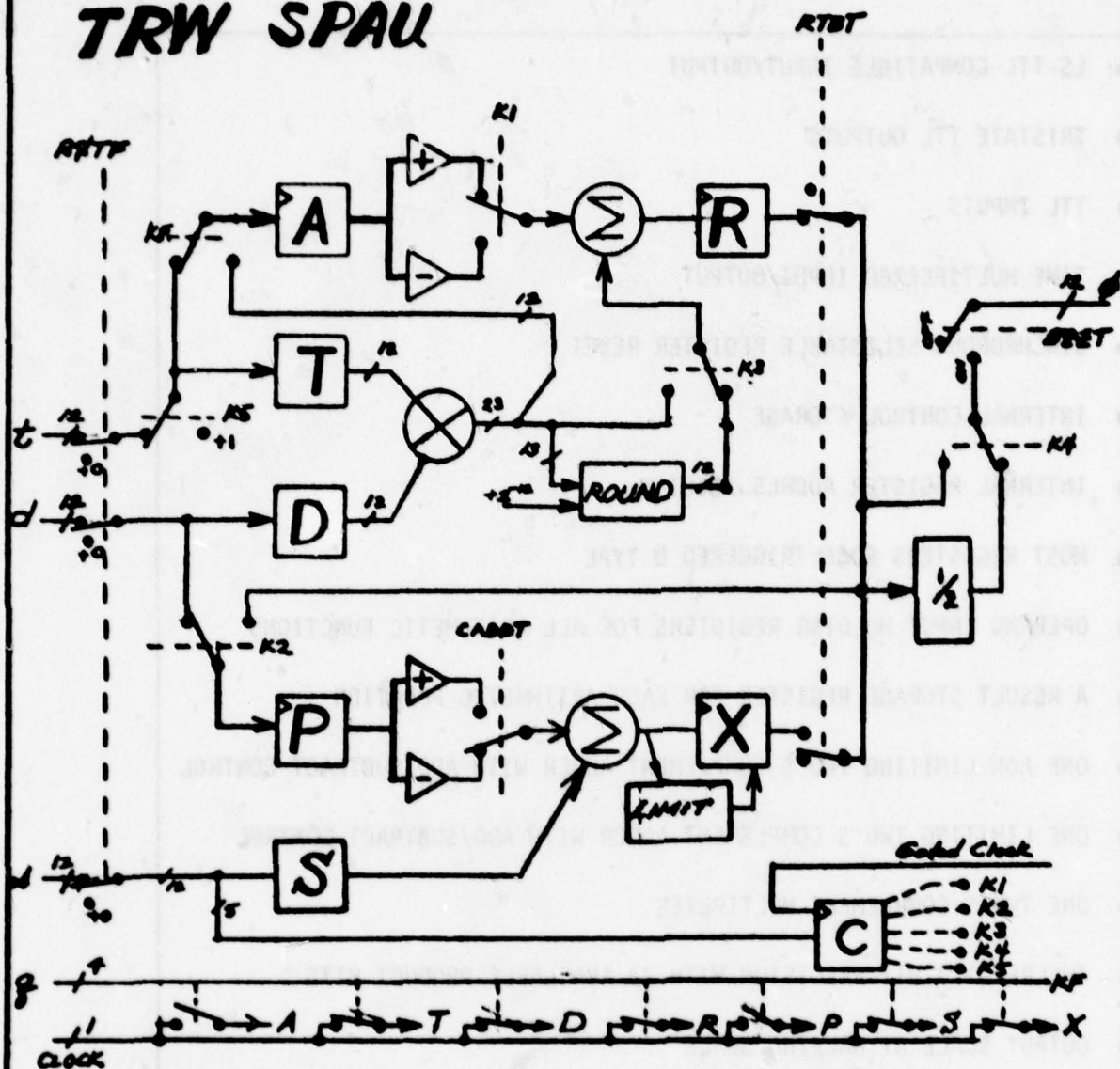
LTR

DESCRIPTION

DATE

APPROVED

TRW SPAU



ENGINEERING SKETCH

ORIGINATOR

Al Whedon

DATE

6/10/75

TRW

SYSTEM GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

Functional Block Diagram

Signal Processing Arithmetic Unit

SIZE

A

CODE IDENT NO.

11982

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Figure 7.

SCALE

SHEET 1 OF

SYSTEMS DES REV. 15/71

TABLE 3. FEATURES OF SPAU 1

- LS-TTL COMPATIBLE INPUT/OUTPUT
- TRISTATE TTL OUTPUTS
- TTL INPUTS
- TIME MULTIPLEXED INPUT/OUTPUT
- SYNCHRONOUS SELECTABLE REGISTER RESET
- INTERNAL CONTROL STORAGE
- INTERNAL REGISTER ADDRESSABILITY
- MOST REGISTERS EDGE TRIGGERED D TYPE
- OPERAND INPUT HOLDING REGISTERS FOR ALL ARITHMETIC FUNCTIONS
- A RESULT STORAGE REGISTER FOR EACH ARITHMETIC FUNCTION
- ONE NON-LIMITING TWO'S COMPLEMENT ADDER WITH ADD/SUBTRACT CONTROL
- ONE LIMITING TWO'S COMPLEMENT ADDER WITH ADD/SUBTRACT CONTROL
- ONE TWO'S COMPLEMENT MULTIPLIER
- TWELVE (12) BIT PRECISION WITH 23 AVAILABLE PRODUCT BITS
- OUTPUT SCALE BY HALF/NO SCALE
- INTERNAL ACCUMULATE FUNCTION ON LIMITING ADDER

3.3 COMPARATIVE ANALYSIS OF SPAU 1 AND SPAU 2 DESIGNS

Two variations of circuit organizations for LSI processing of digital data have evolved. Both of these address the general problem of 12-bit parallel word iterative processing for general purpose digital filtering and FFT in particular. The SPAU 1 was the earlier concept while the SPAU-2 approach was more recently evolved as a simplified architecture approach. The purpose of this analysis is to review both designs on a logical block basis and draw some comparisons. The main equivalence conditions adopted for this analysis is that the operational processing time is the same for both and the LSI packaging constraints in terms of number of pins available are the same; 64 pin DIP packaging is assumed.

3.3.1 Logical Block Diagrams

SPAU 1

The logical block diagrams for the SPAU variations are shown in Figure 8 and Figure 9, respectively. Both of these have four ports for I/O. In the case of the SPAU, three ports (each 12 bits wide) are timeshared inputs feeding six registers. The two main operations performed are multiplication, simultaneous addition/subtraction in the "multiplier" block and disjoint addition/subtraction in the parallel adder/subtractor block. These two main operations can be performed simultaneously with respective outputs stored to two additional registers R and X. The two registers are then multiplexed to the chip output port on demand or internally multiplexed to the P register holding one of the operands interfacing the adder/subtractor. Due to the large number of on-chip registers and controls required most of the clocking and controls are indirect utilizing a four bit clock decode block on the contents of register C provided to store controls required less frequently used (so called slow controls). Also, direct fast controls are available for clock timing, add/subtract control, internal signal mux, round, scale, two input register reset/set over-ride controls, and output tristate.

The basic processing rate of the SPAU 1 is one microcycle period of 120 ns for an Add/subtract and two microcycle periods or 240 ns for a multiply-simultaneous addition. The complexity of the control structure is such as to generally require a pipelined approach to solving an algorithm and obtaining efficient use of the processing capability.

SPAU-2

The SPAU-2 logical block diagram is shown in Figure 9. This is a considerable simplification over the former. Input ports are direct to the registers interfacing the 12-bit parallel multiplier. Two output ports are provided for the least significant product/cumulation and the most significant product/cumulation. All controls are direct. The SUB control either subtracts or adds the contents of the accumulator to the multiplier product for the next microcycle operation. The ACC control enables the accumulation or disables (adds zeros to product) such that the product is available at the outputs or the product/cumulation is available. Note that ACC and SUB are in the feedback loop with the result that no clear or initialization setup is ever required. Four additional bits are available making the total cumulation capacity 27 bits. The typical microcycle period is 175 ns for multiplication/accumulation.

Table 4 shows the salient comparative features of the two organizations from a logical block point of view.

3.3.2 Comparative Advantages and Disadvantages

SPAU

The chief advantage of the SPAU1 organization is one which allows two disjoint operations to go on simultaneously, i.e., multiply/sum and summing operations. In principle, one multiply and three sums can be conducted in 250 ns for a maximum operation rate of $(250/4) = 62.5$ ns per operation. However, this typically can't be sustained in a normal problem algorithm-solving way due to the timeshared terminals and the indirect controls. One particular type of problem, FFT, that has been studied at length shows a practical rate of 192 ns per operation.

The SPAU1 has hardware limiter and scaling provisions. These are necessary due to the limited number field available. The control structure is fairly complicated and the clock decoder has a limited set, 16, of control combinations. This control set can be changed by mask programming to an optimum set for a particular service such as FFT use.

TABLE 4. LOGICAL FEATURES OF SPAU AND SPAU 2
ORGANIZATIONS SIZE AND POWER

ITEM	SPAU	SPAU-2	REMARKS
Input Ports	3, timeshared to 6 destinations	2 direct	
Output Ports	1, internal MUX from 2 sources	2 direct	
Main Operations	D*T \pm A, 250 ns S \pm P, 125 ns	X*Y \neq A, 175 ns	SPAU permits simultaneous operations
Product Significance	SGN +22 SGN +11 MSP, 250 ns SGN +11 LSP, 500 ns	SGN +22, 175 ns	SPAU timeshares' output port for MSP and LSP
Accumulator Significance	SGN +11, 125 ns	SGN +26, 175 ns	Much greater significance for SPAU 2
Hardware Limiting	Yes	No	
Scaler	Yes	No	
Controls	7 direct 13 indirect	9 direct	
Packaging	64 lead DIP	64 lead DIP	
Power	5 watts	2.5 watts	Power reduction, SPAU 2
Device Complexity	15,000 devices	12,000 devices	Reduced complexity, SPAU 2
Chip Size	315 x 351 mils	256 x 256 mils	Smaller chip size, SPAU 2 Smaller package, SPAU 2

SPAU-2

The SPAU-2 organization in contrast to the other, features direct controls and simplicity. Our experience with users is that it is considered preferable perhaps because of just these reasons.

The operational rate of SPAU-2 is a multiply and summation in 175 ns or 88 ns per operation. In the next section several digital filter problem-solving sequences are shown. Using the FFT kernel sequence, 200 ns (worst case) per operation is obtainable. Thus, it compares favorably with the SPAU organization as far as speed goes.

The chief advantage of the new organization other than the simplicity is the extended accuracy available due to the additional four bits of accumulator significance. The SPAU 2 allows double precision arithmetic, yet this is transparent to programming. Also, the LSB's are brought out directly and available without additional sequencing time.

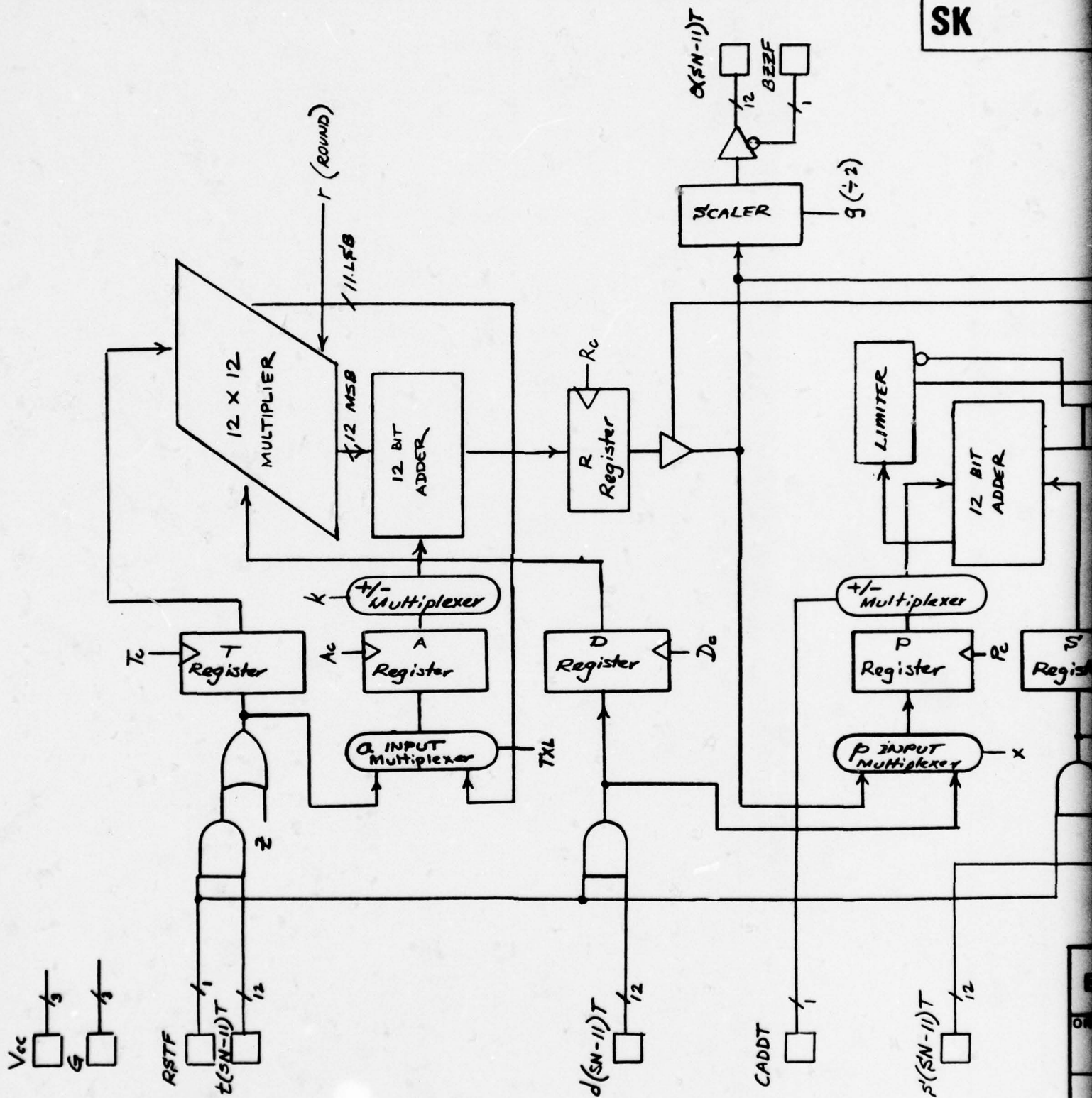
3.3.3 Conclusions on the SPAU Alternatives

The development effort on the SPAU 1 LSI was well spent. It has directly led to extensive circuit development as well as a critical study of alternate architecture concepts and their effectiveness in actual user applications. This study has identified a simplified SPAU architecture called SPAU-2. The simpler approach is clearly the more useful LSI architecture. It has extended accuracy and is more readily understandable and accepted by users. Also, it has less power and the same operational throughput as the original SPAU. The programming is materially simplified.

For these reasons, the SPAU-2 design was adopted over the SPAU 1 implementation. The hardware delivery was completed using this more acceptable design. The -2 chip will directly replace the SPAU in all applications we have studied. A case example is the DFUD (Digital Filter Demonstration Unit) described in Appendix C. Here the -2 can replace the SPAU in the FFT Processor and better augment the output processor in a more efficient way, primarily because of the extended significance of the accumulator requiring materially less supporting chips.

This conclusion and indeed the -2 concept itself is based not only on the studies carried out under the LSI Implementation contract, but through a continued interface with users and potential customers for this type of hardware over the past two years. Therefore, this conclusion is not lightly drawn but believed to be in the best tradition of practical development experience.

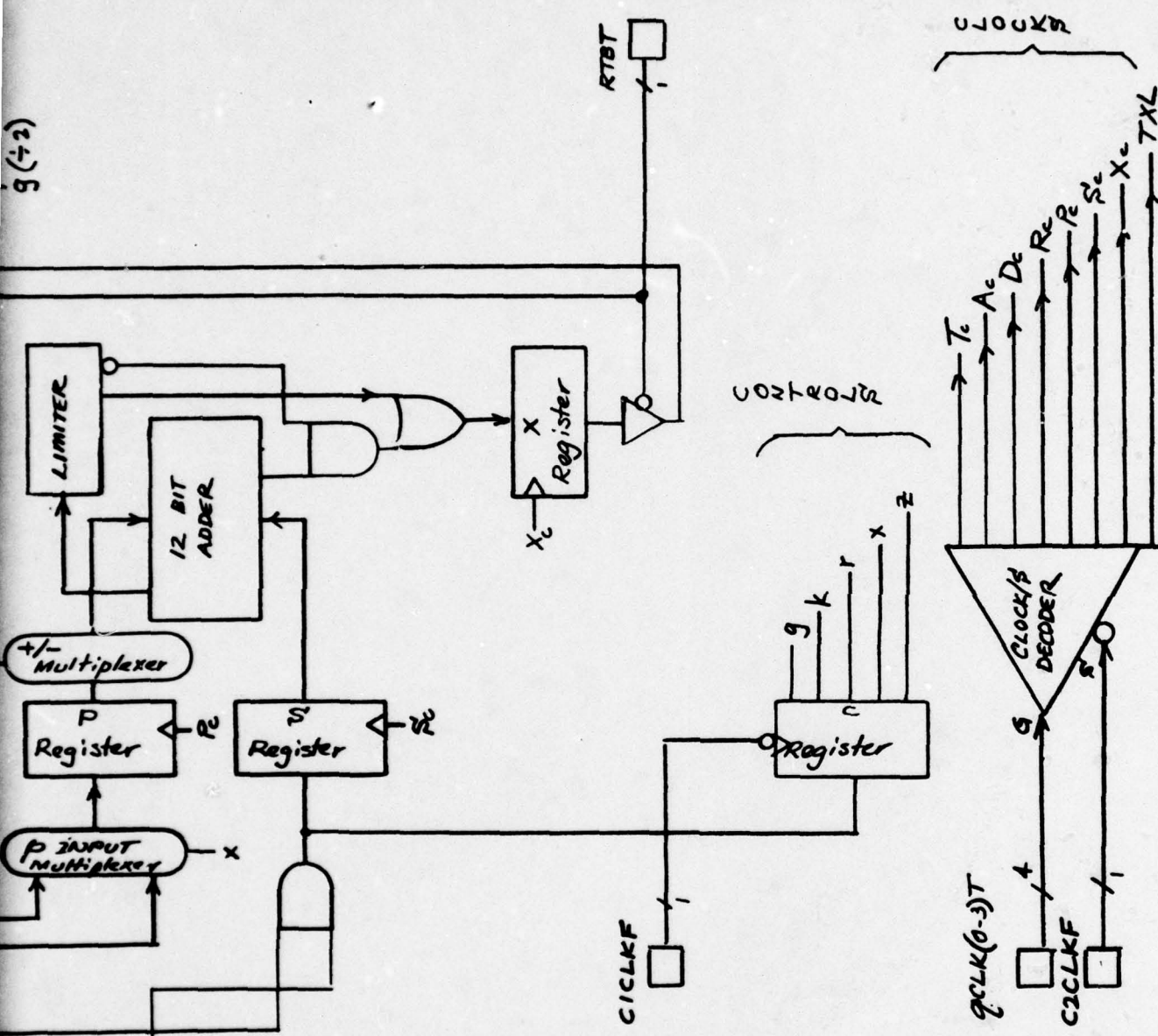
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ENGINEERING SKETCH

ORIGINATOR _____ DATE _____

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

Figure 8.

SPAU1 Block Diagram

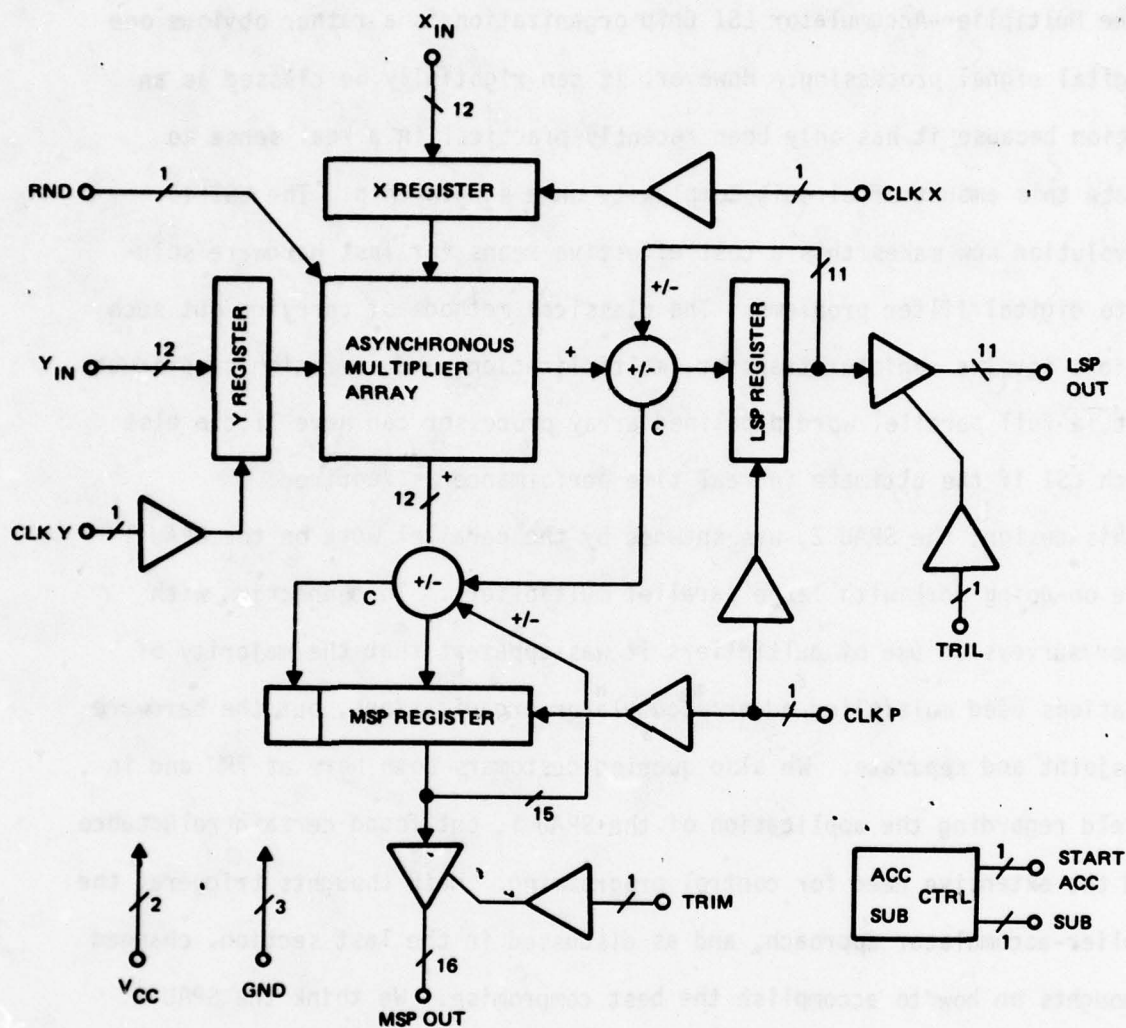
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LOGICAL BLOCK



CONTROLS

CLK X, X_{IN} REGISTER CLOCK

CLK Y, Y_{IN} REGISTER CLOCK

CLK L, LSP REGISTER CLOCK

CLK M, MSP REGISTER CLOCK

TRIL, LSP THREE STATE CONTROL

TRIM, MSP THREE STATE CONTROL

RND, ADDS 2^{-12} TO PRODUCT (FRACTIONAL 2'S COMPLEMENT FIELD)

START ACC, INITIALIZES ACCUMULATOR TO NEXT PRODUCT

SUB, CONTROLS ADDITION/SUBTRACTION

Figure 9. SPAU 2 Logical Block Diagram

3.4 SPAU 2, Multiplier-Accumulator Design

The Multiplier-Accumulator LSI Chip organization is a rather obvious one for digital signal processing. However, it can rightfully be classed as an innovation because it has only been recently practical in a real sense to integrate this amount of circuit complexity on a single chip. The LSI to VLSI evolution now makes this a cost effective means for fast hardware solutions to digital filter problems. The classical methods of carrying out such operations involve register transfer, multiplication, and summation of products. In fact, a full parallel word pipelined array processor can have little else but such LSI if the ultimate in real time performance is required.

This design, the SPAU 2, was spawned by the parallel work on the SPAU 1 and the on-going work with large parallel multipliers. In connection with customer surveys on use of multipliers it was apparent that the majority of applications used multiplier-adder/accumulator organizations, but the hardware was disjoint and separate. We also queried customers both here at TRW and in the field regarding the application of the SPAU 1, but found certain reluctance toward the extensive need for control programming. Main thoughts triggered the multiplier-accumulator approach, and as discussed in the last section, changed our thoughts on how to accomplish the best compromise. We think the SPAU 2 represents this.

In this section, we discuss the design and follow by showing the use of the LSI chip in typical digital filter applications.

The simplified block diagram for the SPAU 2 is shown in Figure 10.

Two inputs X and Y are shown at the top. These are TTL level inputs, each accepting 12 bit two's complement numbers in parallel. These are clocked into input registers using separate clock signals.

The input registers interface directly with the 12x12 bit parallel multiplier. This is an asynchronous logic array which computes continuously producing a 24 bit product. (Sign followed by 23 bits, see I/O number format.) So, as soon as new operands are clocked into the input registers, the multiplication sequence starts. At the product edges of the multiplication array an additional set of adders is provided. The 24 bit product is increased to 27 bits in significance by extending the sign into the higher order bits. The 27 bit adder then accepts directly the product and a 27 bit number from the output register. The output from the adder is directly connected to the 27 bit output register/accumulator. A 27 bit output under 3-state control is buffered to TTL output levels. Two 3-state controls are provided and explained later in the text. **Figure 11 is an expanded block diagram and Figure 12 are the I/O specifications for the SPAU-2.**

Two controls are provided to allow either a straight multiplication mode or the multiplication-accumulation mode. The Accumulate control in the high state passes the output signal to the adder, and the contents of the output register (from the previous operation) are added to the new X, Y product. When the ACC control is in the low state, logic zeros are fed back to the adder disabling the accumulate mode and allows the product only to be captured by the output register/accumulator.

The second control, Add/Sub, is only active in the ACC mode. This control either adds or subtracts the contents of the output register to the next summation cycle. In keeping with 2's complement arithmetic, when subtracting the feedback signals are complemented and a logic 1 is introduced into the LSB position of the adder.

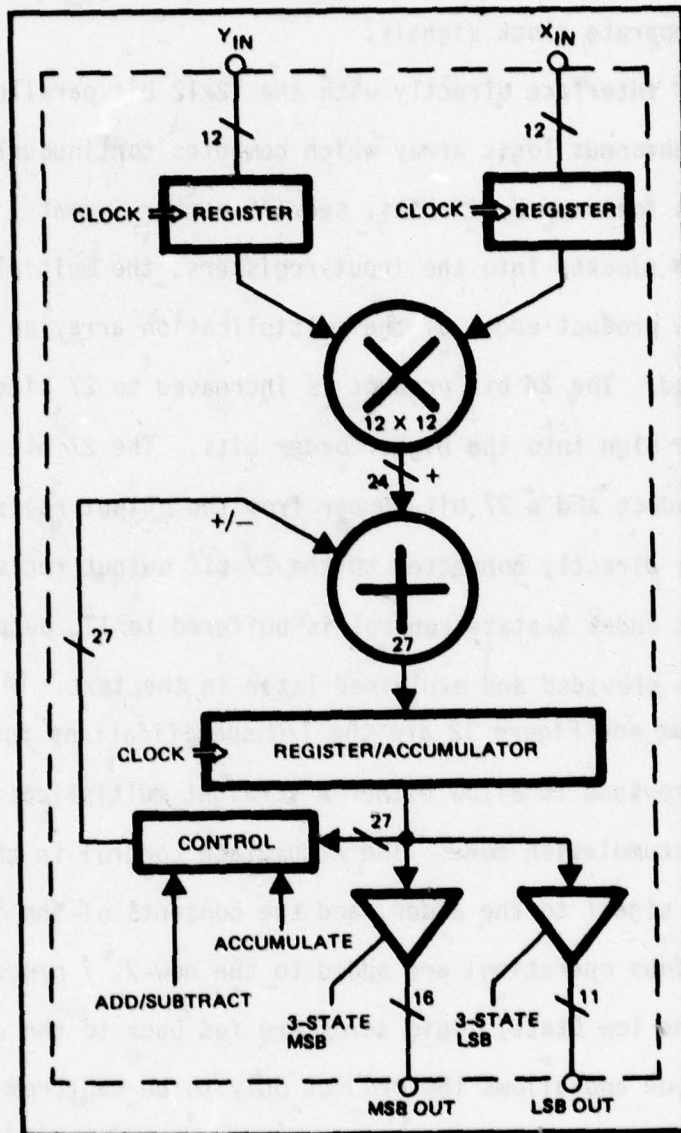
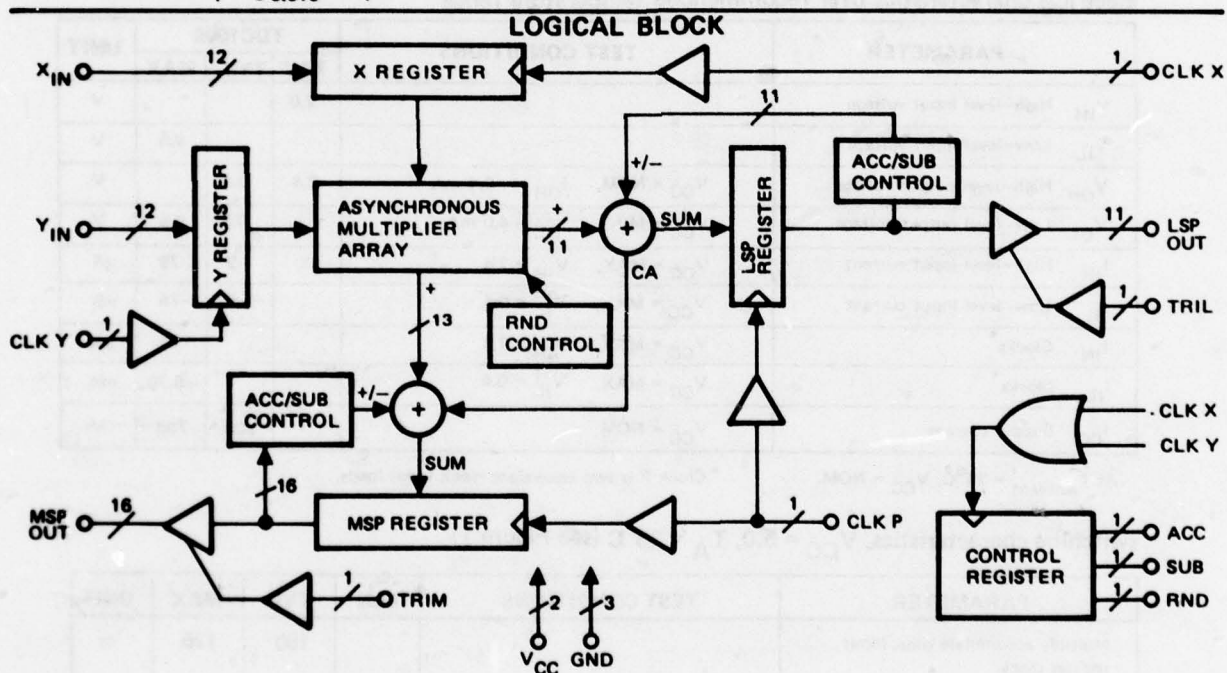
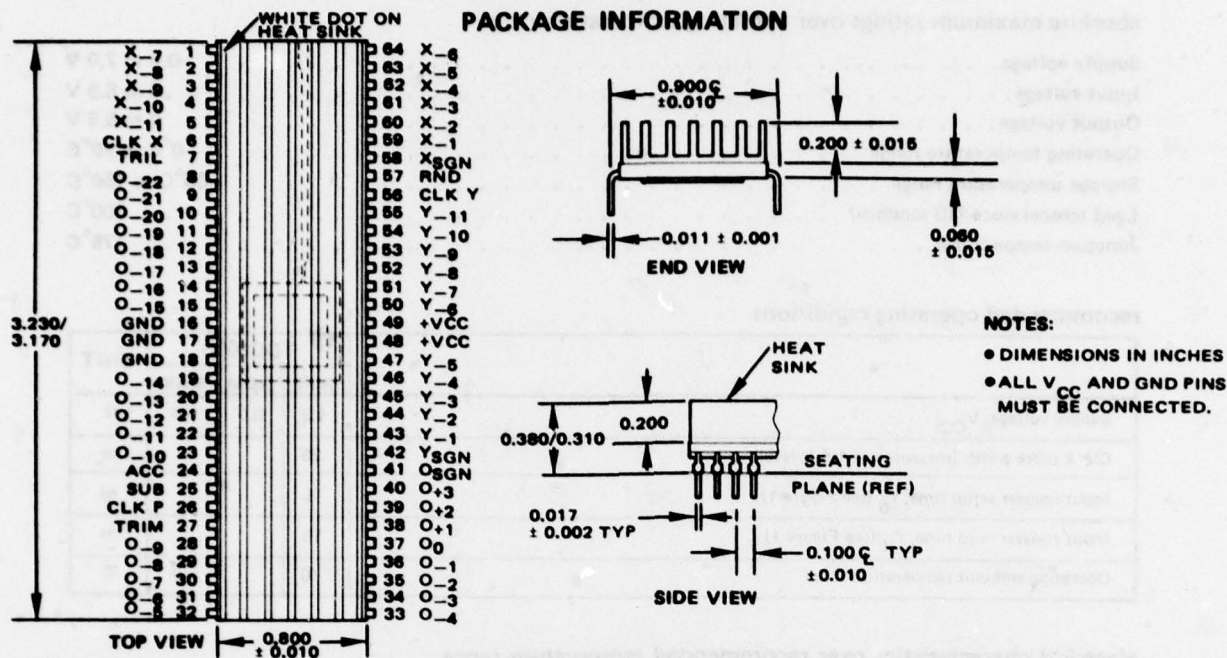


Figure 10. Multiplier-Accumulator Simplified Block Diagram



CONTROLS

CLKX, X_{IN} REGISTER CLOCK } REGISTER CLOCK FOR RND, ACC, AND SUB IS (CLK X + CLK Y)
 CLKY, Y_{IN} REGISTER CLOCK }
 CLK P, OUTPUT REGISTER CLOCK
 TRIL, LSP THREE STATE CONTROL
 TRIM, MSP THREE STATE CONTROL
 RND, ADDS 2^{-12} TO PRODUCT (FRACTIONAL 2S COMPLEMENT FIELD)
 ACC, ENABLES ACCUMULATOR MODE
 SUB, CONTROLS ADDITION/SUBTRACTION OF ACCUMULATOR CONTENTS

Figure 11. Expanded Block Diagram and Packaging Information

absolute maximum ratings over operating temperature range

Supply voltage	-0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

recommended operating conditions

	TDC1003			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5.0	5.5	V
Clock pulse width (measured at 1.5 V level)	25			ns
Input register setup time, T_S (see Figure 1)	5			ns
Input register hold time, T_H (see Figure 1)	15			ns
Operating ambient temperature	0		70	°C

electrical characteristics over recommended temperature range

PARAMETER	TEST CONDITIONS	TDC1003			UNIT
		MIN	TYP	MAX	
V_{IH} High-level input voltage		2.0			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	$V_{CC} = \text{NOM}, I_{OH} = -0.4 \text{ mA}$	2.4	2.7		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 4.0 \text{ mA}$		0.3	0.5	V
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_{IH} = 2.4$		-2	75	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_{IL} = 0.4$		-5	-75	μA
I_{IN} Clocks*	$V_{CC} = \text{MAX}, V_{IH} = 2.4$			75	μA
I_{IL} Clocks*	$V_{CC} = \text{MAX}, V_{IL} = 0.4$			-0.75	mA
I_{CC} Supply current	$V_{CC} = \text{NOM}$		500	750	mA

At $T_{\text{ambient}} = 25^\circ\text{C}$, $V_{CC} = \text{NOM}$.

* Clock P is two equivalent clock input loads.

switching characteristics, $V_{CC} = 5.0$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multiply accumulate time, input register clock To output register clock, T_{MA}			150	175	ns
Output delay T_D			40	50	ns
Three state output delay Output enable Output disable			40 30	50 40	ns ns

Figure 12. SPAU 2 Specifications

The multiplication/accumulation cycle is terminated when the output register is clocked. The complete cycle is measured from input clock to output clock, a period of 175 ns under worse case room temperature conditions. At 75°C ambient temperature the worse case period is 200 ns for the SPAU-2. Continuous operation at this 5 MHz rate can be maintained. The controls ACC and Add/Sub must be held in the same state over the multiplication/accumulation cycle; consequently, these signals are registered and clocked with the input register clock signals. Either CLKX or CLKY, whichever was last, holds the control state. Logically, this is a CLKX OR CLKY signal.

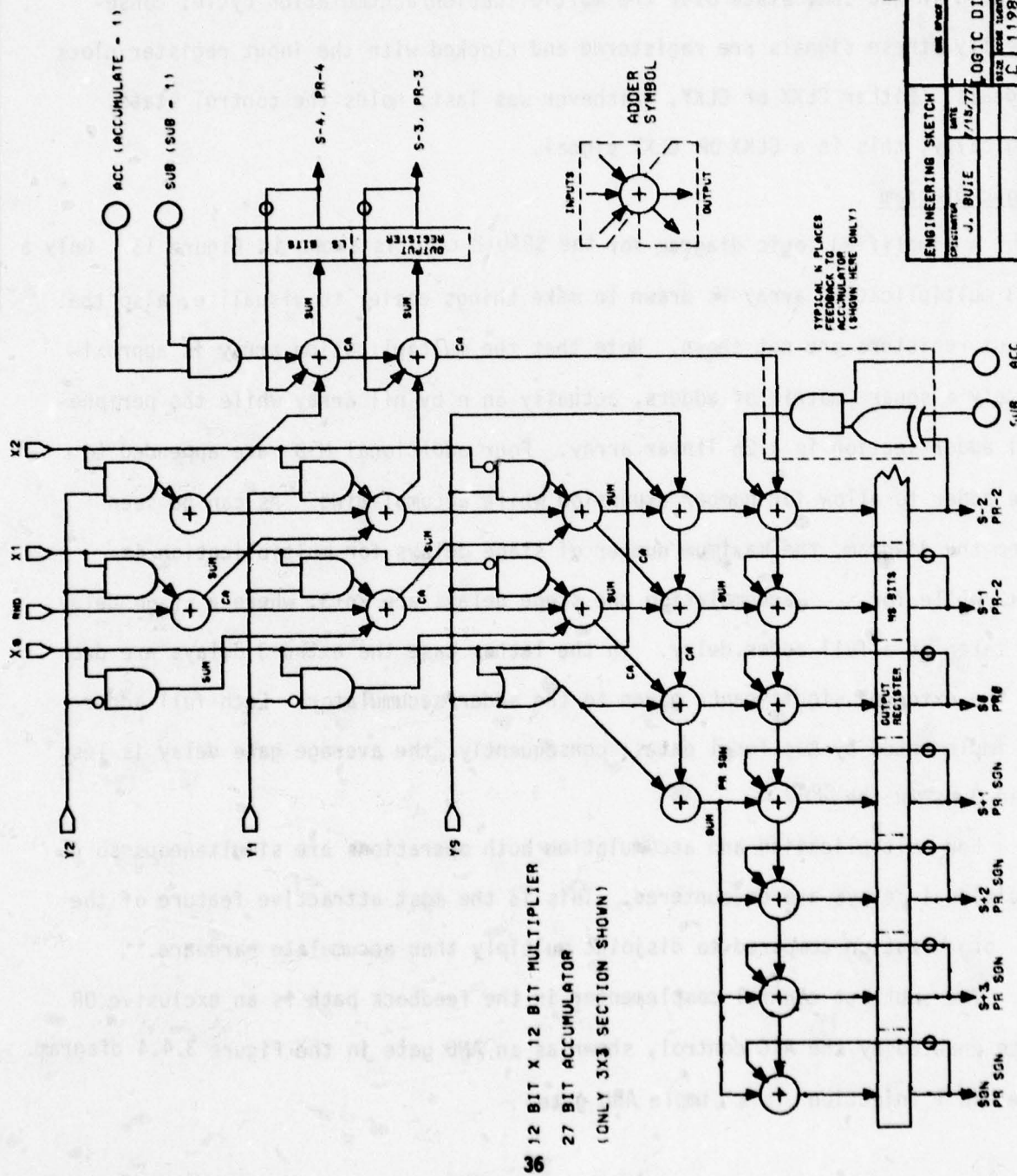
Logic Diagram

A simplified logic diagram for the SPAU 2 chip is shown in Figure 13. Only a 3x3 multiplication array is drawn to make things easier to visualize, also the input registers are not shown. Note that the multiplication array is approximately a square matrix of adders, actually an n by $n+1$ array while the peripheral adder section is a $2n$ linear array. Four additional MSB are appended to the adder to allow for number expansion while accumulating. As can be seen from the diagram, the maximum number of stage delays for multiplication is $2n+2$ while for accumulation the stage delays are $2n+3$, where a stage delay is taken as a full adder delay. In the latter case the extra 3 delays are due to the extended significance given to the adder/accumulator. Each full adder is implemented by two level gates; consequently, the average gate delay is less than 3 ns in the SPAU 2.

For multiplication and accumulation both operations are simultaneous so no additional delays are encountered. This is the most attractive feature of the organization compared to disjoint multiply then accumulate hardware.

The subtract control complementer in the feedback path is an exclusive OR gate enabled by the ACC control, shown as an AND gate in the Figure 3.4.4 diagram. The LSB 1 injection is a simple AND gate.

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ENGINEERING SKETCH	DATE	DESIGNED BY	DATE	CHKD BY	DATE
J. BUJE	7/15/77	TDC1003			
LOGIC DIAGRAM(SIMPLIFIED)					
SIZE 11982 SK					

A third input signal not discussed before is the RND control. The RND control injects a logic 1 into the multiplier array at bit significance 2^{-12} using 2's complement fractional notation. Although injected into the multiplier array, the X and Y operands do not operate on the RND signal. It always adds 2^{-12} to the product. The purpose of this will become apparent after we discuss the output provisions. The RND control like the other controls must be held stable through the multiplication cycle so it is registered and clocked by input clocks CLKX or CLKY, whichever was last.

It is anticipated that a number of users may want to use smaller number fields than 12 bits for both X and Y inputs. In these cases, the prescribed number of bits are connected to the lessor significance bit positions and the sign is extended in the MSB positions. This is easily accomplished by hardwiring the higher order inputs to the sign. Input buffers are provided on all inputs which exhibit very low external drive source and sink requirements. Although the input circuits are TTL compatible the source and sink current requirements are typically less than 10 μ amps. Consequently, no appreciable increase in load is incurred by hardwiring the sign extended bits.

Figure 11 illustrates the division of the 27 bit output register into two parts, a most significant product (MSP) part and an LSP part. The MSP part is 16 bits long and has a separate 3-state control, TRIM. The LSP part is 11 bits long and 3-state control TRIL enables the output (the outputs are enabled when these controls are logic "0"). Many users may only need the MSP for single precision operation and a 16 wide data bus is commonly used; consequently, the 3-state controls were selected this way. The LSP outputs can be hardwired to the same bus if desired. For that matter, all inputs and outputs can be placed on the same bus if desired and time shared by use of the 3-state controls and the input register clock controls. This feature which is common to

TRW's LSI product line has enjoyed a good deal of user acceptance for all parallel iterative processing. A small amount of overhead time sufficient to sequentially load the two input registers is required when operated in this single bus mode.

Returning to the RND control, when in the logic 1 state this adds 2^{-12} to the product/accumulation. Checking with the number field format shown in this article, it is seen that this rounds off the MSP when using single precision results and reduces the truncation error. However, this is only true if the operands used have 12 bit number fields. If this feature is to be preserved for smaller input number fields, then the inputs should be "left justified" (sign occupying the chip sign position and zero filling the right hand remaining positions) instead of the sign extended connection mentioned above. A few moments reflection on the matter should convince you of the rationale for this.

A cell layout diagram of the SPAU 2 is shown in Figure 14. The actual cell layout has almost one-to-one correspondence with the block diagram. The AX labeled cells are full adders which form the main multiplier array. Variations on the full adder cell surround the central core. The adder/accumulator cells labeled ACL and ACM are shown on the right side and bottom. Input and output registers interface directly with I/O bonding pads around the periphery. So, not only in circuit practice, but in actual device layout practice this multiplier/accumulator combination works out to be superbly simple. Additional circuit cells used in the SPAU 2 over these in SPAU 1 are shown in Appendix D.

The chip size is 256 x 256 mils (6.4 x 6.4 mm) and has 64 leads including five for power and ground. The typical power dissipation is 2.5 watts. With this power and number of leads a 64 lead DIP package with an integral heat sink is employed. Operation in still ambient air / ^{with the case temperature at} 125°C for the military version of the MAC12 is practical without any additional thermal crutches. The number of transistors and resistors implementing this chip is approximately 13,000. A microphotograph of SPAU 2 is shown in Figure 15.

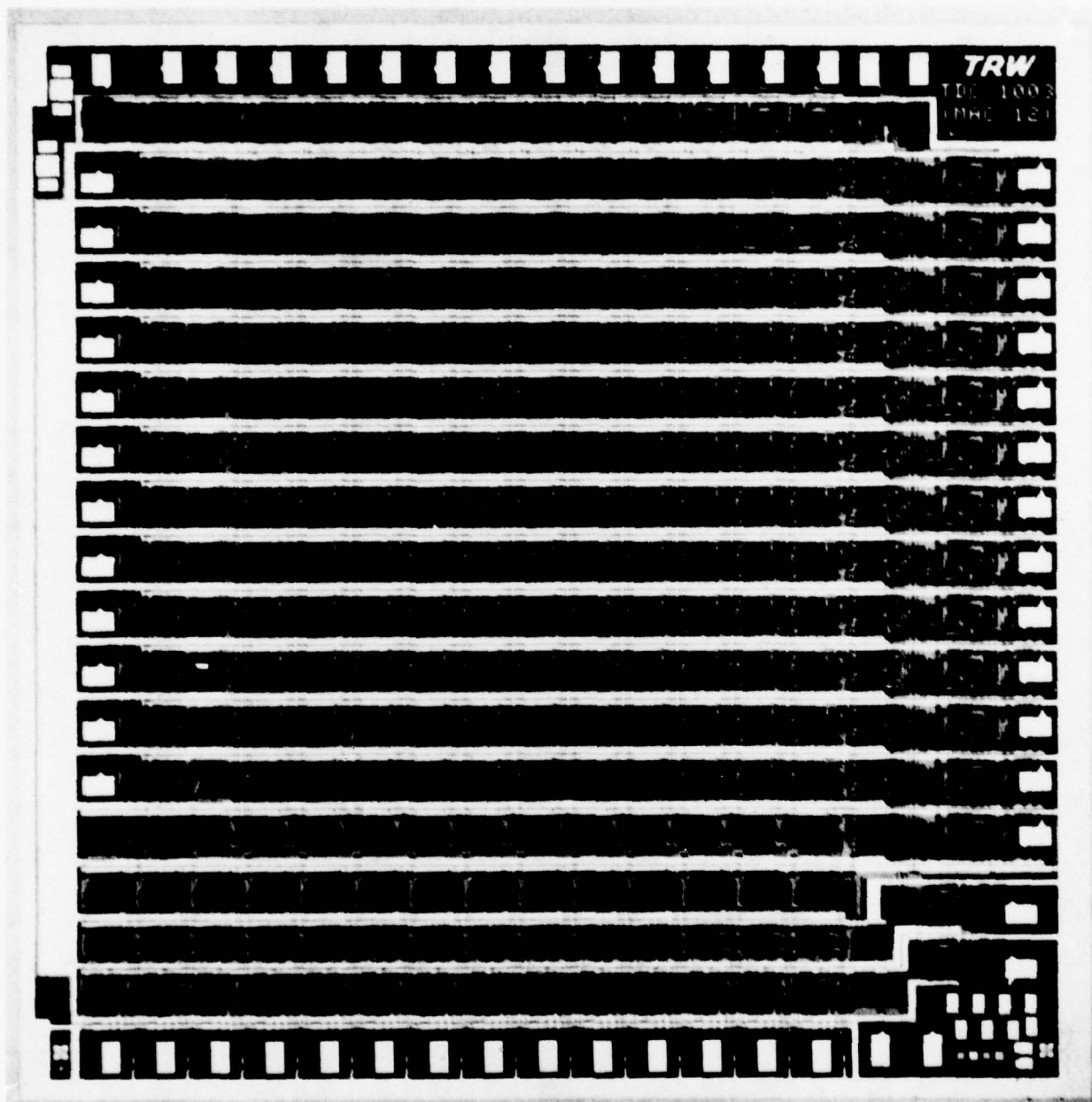


Figure 15. Microphotograph of TDC 1003 (#141212-77)

3.5 SPAU 2 Typical Application

In this section several typical applications of the SPAU 2 are examined. These, of course, represent a small subset of cases where the chip can be used to advantage. Most of the examples take cases where repetitive high speed arithmetic is to be performed using a minimum of off chip control signals.

It is interesting to note the new freedom the multiplier/accumulator offers to digital processing methods. When reviewing the literature on the subject one is struck with the fact that algorithm methods invariably follow the practice of eliminating as much multiplication processes as possible in preference for add/subtract. With the SPAU 2 both multiplication and simultaneous addition/subtraction is the built-in feature representing the best utilization of hardware for maximum operational throughput. Therefore we suspect there is a large body of untapped utility that the multiplier/accumulator organization offers to the filter algorithm field. The availability of this first product innovation should provide the spark to promote more efficient means for its utilization.

In this section we first explore the fundamental operations permissible with SPAU 2 and then extend these to several cases of sequences typically used for digital filtering problems.

A second very important feature is the question of retaining adequate accuracy against scaling and truncation errors. Error analysis shows that in most practical filter systems a 12-bit number scheme can be used if close attention to programming and double precision arithmetic is carried through-out. The SPAU 2 does all operations using full double precision yet this feature is almost transparent to the user. Programming is greatly simplified.

3.5.1 Use of SPAU 2 in the Multiplier Mode

To emphasize principle features of the chip, we take as the first case one where accumulation is not desired and the operation is multiplication only. This is also the mode used for initialization of the first step used in a sequence of multiplication/accumulation. The format, shown in Table 5, lists the states of the control signals prior to clocking the input/output registers. A single system clock signal is assumed where there is a small but defined source/transmission delay between the source of the operands and clock inputs to the chip. The operand source delay plus the transmission must be greater than 10 ns and less than $\tau_{ma} - \tau_s$, where τ_{ma} is the multiplication/accumulation period and τ_s is the input register set-up time. This is a conventional type of consideration for D type register elements and guarantees maximum operating speed.

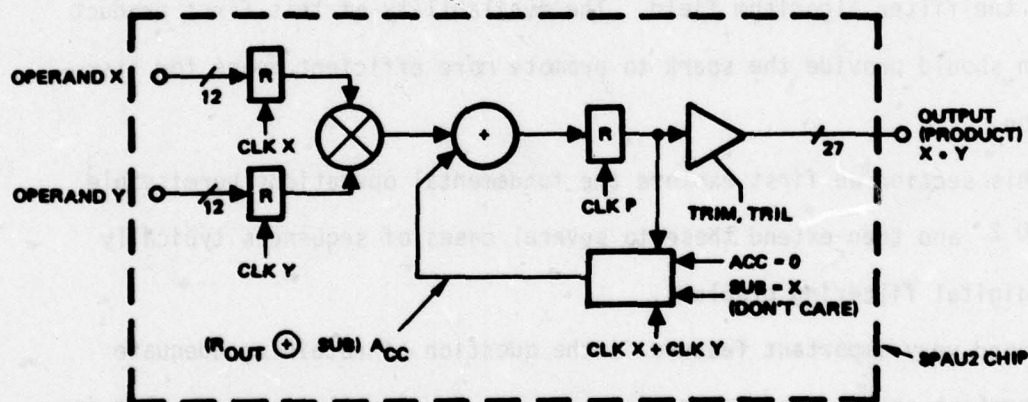


Figure 16. Setup for Multiplication

Figure 16 shows the connections for the SPAU-2 when operating in the multiplication mode only. Table 5 shows the control states and operating sequence. Steps 1 through 4 illustrate a typical iterative multiplication procedure showing a new product available at the output registers after each 200 ns.

TABLE 5. CONTROL STATES AND OPERATING SEQUENCE, MULTIPLIER MODE

REF STEP	INPUT DATA		CONTROLS							OUTPUT DATA		CUMULATIVE TIME
	X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	CONTENTS OF OUTPUT REGISTER	
1	X_1	Y_1	0	0	0	\square	\square	0	0	0	(PREVIOUS OPERATION)	0
2	X_2	Y_2	0	0	0	\square	\square	\square	0	0	$X_1 \cdot Y_1$	200
3	X_3	Y_3	0	0	0	\square	\square	\square	0	0	$X_2 \cdot Y_2$	400
4	X_4	Y_4	0	0	0	\square	\square	\square	0	0	$X_3 \cdot Y_3$	600
	— ETC —											
5	X_i	Y_i	0	0	1	\square	\square	\square			$X_{i-1} \cdot Y_{i-1}$	-
6	X_{i+1}	Y_{i+1}	0	0	0	\square	\square	\square	0	0	$X_i \cdot Y_i + 2^{12}$	-
7	X_{i+2}	Y_{i+2}	0	0	0	\square	\square	\square	0	0	$X_{i+1} \cdot Y_{i+1}$	-
8	X_j	$(1 \cdot 2^{22})$	0	0	0	\square	\square	0	0	0	(PREVIOUS OPERATION)	-
9	X_j	-1	0	0	0	\square	\square	\square	0	0	$X_j \cdot (1 \cdot 2^{22})$	-
10	$(1 \cdot 2^{22})$	Y_j	0	0	0	\square	\square	\square	0	0	$-X_j$	-
11	-1	Y_j	0	0	0	\square	\square	\square	0	0	$Y_j \cdot (1 \cdot 2^{22})$	-
12	-	$-Y_j$	0	0	0	0	\square	\square	0	0	$-Y_j$	-
13	-	-1	0	0	0	0	\square	\square	0	0	Y_j	-
14	-	-	-	-	-	0	0	\square	0	0	1	-

The ACC control is held at logic zero for this mode which disables the feedback to the adder. The outputs to the package pins go through the 3-state TTL buffer under the TRIM and TRIL controls. TRIM is the 3-state control for the 16 MSP outputs and TRIL is the 3-state control for the 11 LSP outputs. Logic zero state for TRIM and TRIL enables the outputs to the low impedance TTL level states. In case one were to time share the outputs to the same bus, then TRIM and TRIL would be used to first read one portion of the product out to the bus and then the other.

The sequence in Table 5 under steps 5 through 7 shows the result of using the RND control in step 5. As shown in step 6 this adds the quantity 2^{-12} (two's complement fractional notation) to the product. Typically, RND would only be used if one were outputting the MSP and wanted to "round" and thereby reduce the error introduced by truncation.

One of the basic operations of transferring a number from the input of SPAU 2 to the output is the special case of multiplication where the coefficient is unity. This is illustrated in Table 5 under steps 8 through 13. Scaling and negation are also similar operations which use an appropriate coefficient for the multiplier. The notation we have adopted for the two's complement numbers is to treat the number field as fractional with the binary point located immediately after the sign bit (for numbers input to the multiplier). With this notation a true +1 unity value is not quite available and the closest quantity to it is $(1*2^{-11})$. On the other hand, a true -1 of unity absolute value is available and this will negate the input variable exactly and transfer to the output as shown in either steps 12 or 13. For those of you who are not 2's complement buffs you may want to review the format notes shown at the end of this section. For those of you who are, we show step 14 where $-1*-1 = 1$ which is permissible in the SPAU 2 because extended significance is provided by additional adders in the output circuits.

Once an operand is loaded into the input register by the respective input clock the value will be held until changed. This is illustrated in steps 11 through 14. This concludes the multiplier features and we examine next the accumulator mode.

3.5.2 Use of SPAU 2 in the Accumulator Mode

Table 2 illustrates the multiplier/accumulator mode for the SPAU 2. We take as a first case a simple counter where the modulus is $(X_1 * Y_1)$. Note in line 1 that the only initialization procedure is to place the ACC control at logic 0 and at t_{ma} time later (200 ns) the first count value $(X_1 * Y_1)$ is available at the output register. At step 2, ACC=1 is loaded into its holding register. Successive accumulation of the counting modulus is shown in steps 3 and 4.

The effect of the SUB control is shown in steps 4 and 5. SUB, negates the number fed back to adder. Consequently, the numbers added are $(X_1 * Y_1) - 3(X_1 * Y_1) = -2(X_1 * Y_1)$. Positive accumulation is then restored at step 5 and the count proceeds in ascending order to zero at step 7.

In Table 6 the dash marks are a "don't care" state. The controls ACC, SUB, and RND are registered controls loaded by CLKX or CLKY. TRIM and TRIL do not effect the internal operation.

Steps 8 through 13 show the solution of an arbitrary function:
 $F(X, Y, Z, K) = X^2 - Y^2 + Z^2 + KZ - K$. This would normally take 4 additions and 4 multiplications, whereas the SPAU 2 does this in 5 steps of 200 ns each; thus, computing the function in one microsecond yielding a full double precision result.

TABLE 6. MULTIPLIER/ACCUMULATOR MODE

INPUT DATA			CONTROLS								OUTPUT DATA	
REF STEPS	OPERAND X	OPERAND Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	CONTENTS OF OUTUPT REGISTER	
1	X ₁	Y ₁	0	0	0				0	0	(PREVIOUS OPERATION)	
2	.	Y ₁	1	0	0	0			0	0	(X ₁ * Y ₁)	
3	0	0		0	0	2 (X ₁ * Y ₁)	
4	X ₁	.	1	1	0		0		0	0	3 (X ₁ * Y ₁)	
5	X ₁	.	1	0	0		0		0	0	-2 (X ₁ * Y ₁)	
6	0	0		0	0	-(X ₁ * Y ₁)	
7	0	0		0	0	0	
8	Y	Y	0	0	0				0	0	(X ₁ * Y ₁)	
9	X	X	1	1	0				0	0	Y ²	
10	Z	Z	1	0	0				0	0	X ² . Y ²	
11	.	K	1	0	0	0			0	0	X ² . Y ² + Z ²	
12	.1	.	1	0	0		0		0	0	X ² . Y ² + Z ² + KZ	
13	0	0		0	0	X ² . Y ² + Z ² + KZ . K	

0
200
400
600
800
1000 ns

3.5.3 Example for Numerical Integration

Based on the area under a parabolic arc, Simpson's rule is an accepted method for numerical integration of a sampled data sequence.

Let a function $y(t)$ be sampled at $n + 1$ points, such that y_0, y_1, \dots, y_n are equally spaced at an incremental interval T . Assume that n is even. Then according to Simpson's rule (see almost any calculus textbook), the area A_S under the curve $y(t)$, given by

$$A_S = \int_{t_1}^{t_1 + nT} y(t) dt, \quad (1)$$

may be approximated by

$$A_S = \frac{T}{3} (y_0 + 4y_1 + 2y_2 + 4y_3 + 2y_4 + \dots + 4y_{n-1} + y_n). \quad (2)$$

This is generally more accurate than the so-called trapezoidal rule

$$A_T = \frac{T}{2} (y_0 + 2y_1 + 2y_2 + \dots + 2y_{n-1} + y_n), \quad (3)$$

which approximates the function $y(t)$ by straight-line segments and therefore fails to take account of curvature.

An accumulation of the terms in Equation (2), therefore, implements Simpson's rule explicitly, where it is necessary only to input the sequence of sampled points and the appropriate sequence of weighing coefficients. After any step m , where $m < n$, the contents of the accumulator are \bar{A}_m , which is an approximation to the running integral up to that point. When $m = n$ and the accumulation is terminated with the proper weighting coefficient (see Note), the evaluation is complete and $\bar{A}_n = A_S$.



Figure 17. Numerical Integration

TABLE 7. SEQUENCE FOR NUMERICAL INSERTION

INPUT		CONTROLS								OUTPUT REGISTER
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	
y_0	$T/3$	0	0	0			0	0	0	
y_1	$4T/3$	1	0	0				0	0	$y_0 T/3$
y_2	$2T/3$	1	0	0				0	0	$y_0 T/3 + 4y_1 T/3$
y_3	$4T/3$	1	0	0				0	0	$y_0 T/3 + 4y_1 T/3 + 2y_2 T/3$
y_n	$T/3$	1	0	0				0	0	
-	-	-	-	-				0	0	$\bar{A} = F(T_2 Y)$

NOTE: To avoid termination error, based on Simpson's rule outlined above, the integration should terminate on an odd number of samples (n even) with a weight of $T/3$, as shown. If it is necessary to terminate on an even number of samples (n odd), then it is a good approximation to keep the sequence up to that point and terminate with a weight of $2T/3$.

3.5.4 Example for Complex Multiplication

Given two complex numbers Z_1 and Z_2 and multiplying these we have

$$Z_1 = X_1 + jY_1$$

$$Z_2 = X_2 + jY_2$$

$$Z_1 * Z_2 = X_1 * X_2 - Y_1 * Y_2 + j(X_1 * Y_2 + X_2 * Y_1)$$

$$= X + jY$$

A diagram for this operation is shown in Figure 18.

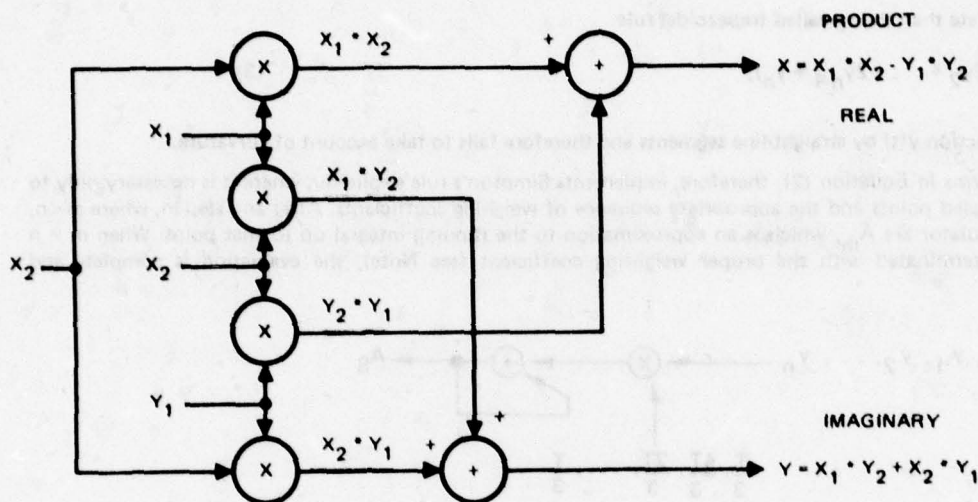


Figure 18. Complex Multiplication

TABLE 8. SEQUENCE USING ONE SPAU 2

INPUT		CONTROLS								OUTPUT TERMINALS	NS
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL		
Y_1	Y_2	0	0	0			0 1	1	1	-	0
X_1	Y_2	1	1	0				1	1	-	200
X_1	Y_2	0	0	0				0	0	$X = X_1 * X_2 - Y_1 * Y_2$	400
X_2	Y_1	1	0	0				1	1		800
-	-	-	-	-	0	0		0	0	$Y = X_1 * Y_2 + X_2 * Y_1$	300

To compute this using disjoint adder-multiplier means requires 4 multiplications and 2 additions for 6 operations. Here we see that one SPAU 2 in four steps computes the complex product in 800 ns. It is clear that using two chips, one operating on the reals and the other the imaginaries, would compute in 400 ns.

3.5.5 Example for Discrete Fourier Transform Solution

Solution of the DFT was shown in Section 2.2. The connections and tabular listing of the controls are quite simple with the SPAU 2. These are shown in Table 9 and the diagram Figure 19.

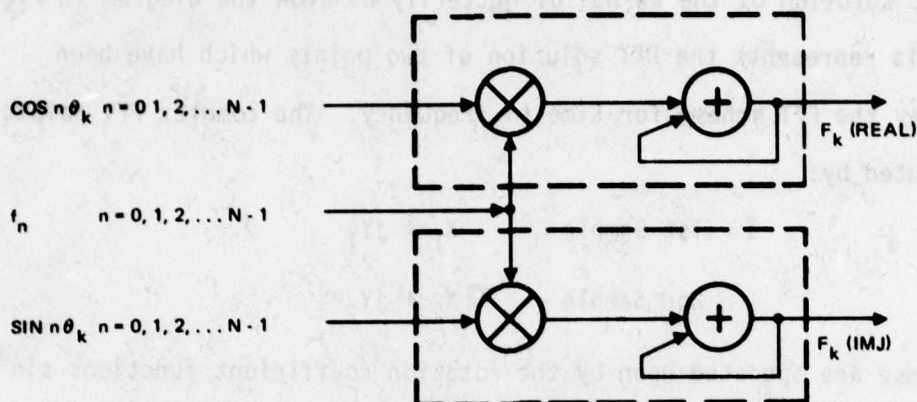


Figure 19. Reals Solution Only, Imaginary Solution is Similar, DFT

TABLE 9. DFT SEQUENCE

INPUT		CONTROLS								OUTPUT REGISTER	NS
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL		
f_0	1	0	0	0				1	1		0
f_1	$\cos \theta_k$	1	0	0				1	1	f_0	200
f_2	$\cos 2\theta_k$	1	0	0				1	1	$f_0 + f_1 \cos \theta_k$	400
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		
f_{N-1}	$\cos (N-1)\theta_k$	1	0	0				1	1	$f_0 + f_1 \cos \theta_k + f_{N-2} \cos (N-2)\theta_k$	
-	-	-	-	-	0	0		0	0	$f_0 + f_1 \cos \theta_k + f_{N-1} \cos (N-1)\theta_k$	N * 200

TRANSFER TO DESTINATION

3.5.6 Example for Computing the Kernel in Solution of the FFT Using SPAU 2

The arithmetic operation discussed in section 2.3, solution of the complex arithmetic in connection with FFT problems finds a ready answer using the SPAU 2.

For solution of the kernel or butterfly we show the diagram in Figure 20. This represents the DFT solution of two points which have been paired by the FFT scheme for time to frequency. The complex FFT points are represented by:

$$\text{1st Sample} \quad X_1 + jY_1$$

$$\text{2nd Sample} \quad X_2 + jY_2$$

These are operated upon by the rotation coefficient functions \sin^θ and \cos^θ . The particular solution we are implementing is shown below. The primed quantities represent the transformed values.

$$X_1 + X_2 \cos \theta + Y_2 \sin \theta = X_1 + Z_1 = X'_1$$

$$Y_1 - X_2 \sin \theta + Y_2 \cos \theta = Y_1 + Z_2 = Y'_1$$

$$X_1 - X_2 \cos \theta - Y_2 \sin \theta = X_1 - Z_1 = X'_2$$

$$Y_1 + X_2 \sin \theta - Y_2 \cos \theta = Y_1 - Z_2 = Y'_2$$

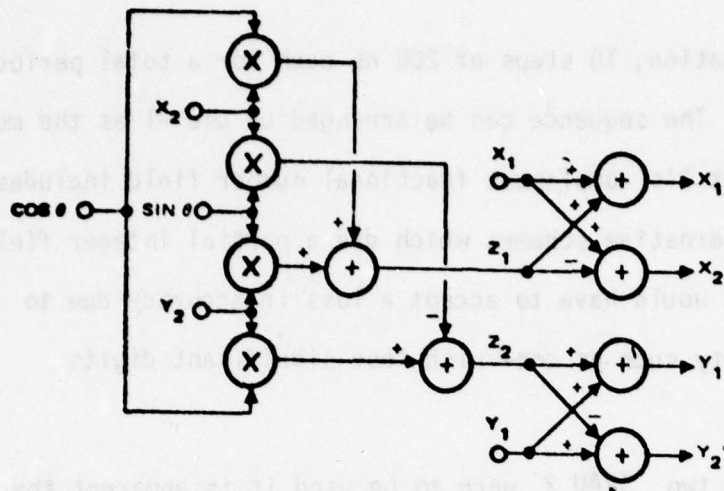


Figure 20. Diagram for Solution of Butterfly

TABLE 10. SEQUENCE FOR KERNEL SOLUTION USING ONE SPAU 2

INPUT		CONTROLS								CONTENTS OF OUTPUT REGISTER
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	
x_2	$\cos \theta$	0	0	0				0	0	
x_2	$\sin \theta$	1	0	0				0	0	$x_2 \cos \theta$
x_1	1	1	0	0				0	0	$x_2 \cos \theta + y_2 \sin \theta$
x_1	1	1	1	0				0	0	$x_1 + x_2 \cos \theta + y_2 \sin \theta - x_1' \sin \theta = x_1'$
x_1	1	1	0	0				0	0	$-z_1$
x_2	$\sin \theta$	0	0	0				0	0	$x_1 - z_1 = x_2'$
y_2	$\cos \theta$	1	1	0				0	0	$x_2 \sin \theta$
y_1	1	1	0	0				0	0	$-x_2 \sin \theta + y_2 \cos \theta$
y_1	1	1	1	0				0	0	$y_1 - x_2 \sin \theta + y_2 \cos \theta - y_1' \cos \theta = y_1'$
y_1	1	1	0	0				0	0	$-z_2$
-	-	-	-	-	0	0		0	0	$-y_1 - z_2 = y_2'$

For this implementation, 10 steps of 200 ns each for a total period of 2 μ s. is required. The sequence can be arranged to use -1 as the multiplier. The twelve bit 2's complement fractional number field includes $1-2^{-11}$ but not 1. Alternative schemes which use a partial integer field also avoid error, but would have to accept a loss in accuracy due to representing a quantity such as $\cos \theta$ with less significant digits.

For the case where two SPAU 2 were to be used it is apparent that only five steps are required, one computing X_1' and X_2' , while the other computes Y_1' and Y_2' .

3.5.7 Non-Recursive Filter Implementation

The DFT and the butterfly are examples of non-recursive filters since the outputs do not operate on the inputs in a feedback mode. More typical cases of non-recursive filter implementation with SPAU 2 are discussed in this section.

The non-recursive filter is shown in Figure 21. This has the transfer function $H(z)$.

$$H(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + h_3 z^{-3}$$

The h 's are weighting coefficients applied to delayed sample data, where z^{-1} represents one sample period delay, z^{-2} represents two sample period delays, etc. The zeros of this transfer function can be found by setting $H(z) = 0$ and solving the polynomial for z . Filters of this type can be used for smoothing noisy data, windowing the DFT, and as a part of more complex filters. A block diagram is shown in Figure 21.

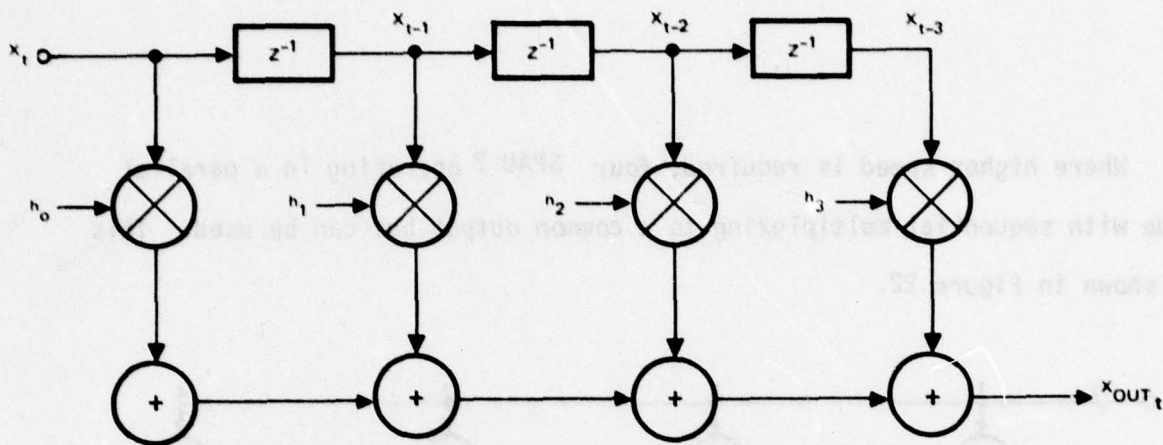


Figure 21. Non-Recursive Filter

To implement the filter using one SFAU 2, the input data x_t is held at one of the inputs for the duration of the filter delay, four periods for the Figure 21 case. Successive operation by the weighting coefficients and cumulation of the products is then stored in the output register. The sequence is shown in Table 11.

TABLE 11. SEQUENCE FOR SOLUTION OF NON-RECURSIVE FILTER

INPUT		CONTROLS								CONTENTS OF OUTPUT REGISTER
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	
x_t	h_0	0	0	0			0	0	0	
x_{t-1}	h_1	1	0	0				0	0	$x_t * h_0$
x_{t-2}	h_2	1	0	0				0	0	$x_t * h_0 + x_{t-1} * h_1$
x_{t-3}	h_3	1	0	0				0	0	$\dots + x_{t-2} * h_2$
x_{t+1}	h_0	0	0	0				0	0	$\dots + x_{t-3} * h_3 = x_{OUT,t}$
x_t	h_1	1	0	0				0	0	$x_{t+1} * h_0$
x_{t-1}	h_2	1	0	0				0	0	$x_{t+1} * h_0 + x_t * h_1$
x_{t-2}	h_3	1	0	0				0	0	$\dots + x_{t-1} * h_2$
ETC	0	0	0	0				0	0	$\dots + x_{t-2} * h_3 = x_{OUT,t+1}$

Where higher speed is required, four SPAU 2 operating in a parallel mode with sequential multiplexing to a common output bus can be used. This is shown in Figure 22.

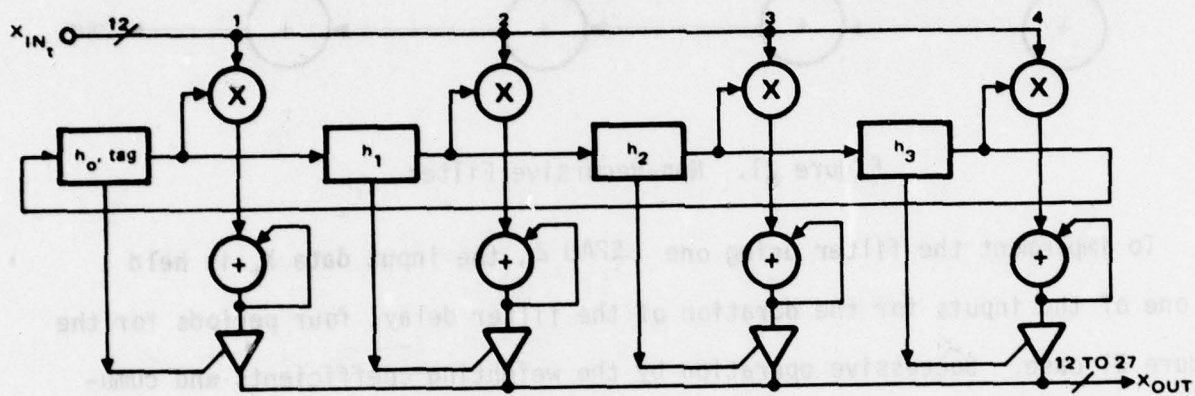


Figure 22. Non-recursive Filter, Parallel Mode

An external four-stage circulating shift register holds the weighting functions, h . A tag bit is also circulated in the h shift registers which operates the 3-state control, thereby busing the accumulator contents to the output in sequence. Input register clocking, output register clocking and h shift register are all operated directly from the 5 MHz system clock. The control ACC is also operated from the tag bit as well as the 3-state control. As can be traced from the block diagram, each SPAU 2 accumulates four products and then is gated to the output bus. On the next clock period the adjacent SPAU 2 is outputted, etc. By these means, steady outputs at the 5 MHz rate are sustained. The latency period is four clock periods or 800 ns. The internal operation sequence for any one SPAU 2 is the same as shown in the previous implementation.

3.5.8 Recursive Filter Implementation

The usual block diagram for the simplest recursive digital filter is shown in Figure 23.

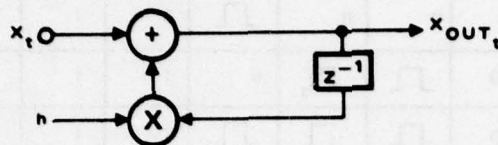


Figure 23. Simple Recursive Filter

The MAC organization has internal feedback for product accumulation but it is not provided with output to multiplier input signal connections which the recursive filter requires. However, externally the output can be bused to the input as shown in Figure 24. The 3 state output controls and the input register clock controls effect time sharing the inputs and outputs.

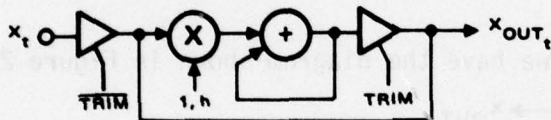


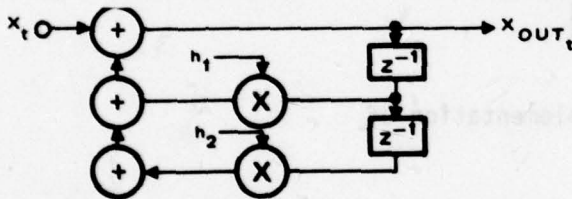
Figure 24. Single SPAU 2 Part Implementation of Single Pole Filter

In this case, two step operation is used where the input into the multiplier is alternated between 1 and weight coefficient h and the output is read out on alternate clock cycles. Operation is shown below, assuming initial output accumulator contents of value ψ . A full multiply period is used to allow transfer from the output to the input. This assumes a single phase clock system is used. More efficient utilization for this type of operation can be realized using a multiphase clock system, however, for simplicity in displaying the sequence and in common with the other sequences presented the single clock method is assumed for the operation shown in Table 12.

TABLE 12. RECURSIVE FILTER OPERATION USING SPAU 2

INPUT		CONTROLS								CONTENTS OF OUTPUT REGISTER
X	Y	ACC	SUB	RND	CLK X	CLK Y	CLK P	TRIM	TRIL	
-	-	-	-	-	0	0		0	1	$X_{OUT_{to}} = v$
v	h	0	0	0			0	1	1	
X_{t+1}	1	1	0	0				1	1	Hv
-	-	-	-	-	0	0		0	1	$X_{t+1} + hv = X_{OUT_{t+1}}$
$X_{OUT_{t+1}}$	h	0	0	0			0	0	1	
X_{t+2}	1	1	0	0				1	1	$h(X_{OUT_{t+1}})$
-	-	-	-	-	0	0		0	1	$X_{t+2} + h(X_{OUT_{t+1}}) =$ $X_{OUT_{t+2}}$
$X_{OUT_{t+2}}$	h	0	0	0				1	1	$h(X_{OUT_{t+2}})$
					ETC					

For a two or more pole filter we have the diagram shown in Figure 25.



$$X_{OUT_{t_0}} = v$$

$$X_{OUT_{t+1}} = X_{t+1} + h_1 v$$

$$X_{OUT_{t+2}} = X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v$$

$$X_{OUT_{t+3}} = X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v] + h_2 (X_{t+1} + h_1 v)$$

$$X_{OUT_{t+4}} = X_{t+4} + h_1 X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v] + h_2 (X_{t+1} + h_1 v) + h_2 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v]$$

In general

$$X_{OUT_t} = X_t + h_1 (X_{OUT_{t-1}}) + h_2 (X_{OUT_{t-2}}) + \dots + h_n (X_{OUT_{t-n}})$$

$$X_{OUT_t} = X_t + \sum_{i=1}^n h_i (X_{OUT_{t-i}})$$

Figure 25. Two or More Pole Recursive Filters

Using the methods outlined the multipole filter as well as poles and zeros combinations can be implemented using the multiplier-accumulation organization.

3.5.9 Number Field Format for SPAU 2

The format used for the number system on SPAU 2 is shown below.

FORMAT: 2'S COMPLEMENT FRACTIONAL NOTATION
(NOTE 3)

X INPUT	X _{SGN}	X ₋₁	X ₋₂	X ₋₃	X ₋₄	X ₋₅	X ₋₆	X ₋₇	X ₋₈	X ₋₉	X ₋₁₀	X ₋₁₁
	SGN	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹

Y INPUT	Y _{SGN}	Y ₋₁	Y ₋₂	Y ₋₃	Y ₋₄	Y ₋₅	Y ₋₆	Y ₋₇	Y ₋₈	Y ₋₉	Y ₋₁₀	Y ₋₁₁
---------	------------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	------------------	------------------

OUTPUT FORMAT WHEN NONACCUMULATING PRODUCTS (ACC = 0) FOR PINOUT DIAGRAM O_n = PR_n

PR SGN +4	PR SGN +3	PR SGN +2	PR SGN +1	PR 0	PR -1	PR -2	PR -3	PR -4	PR -5	PR -16	PR -17	PR -18	PR -19	PR -20	PR -21	PR -22
2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²
SGN	SGN	SGN	SGN													

NOTE 1

OUTPUT FORMAT WHEN ACCUMULATING PRODUCTS (ACC = 1) FOR PINOUT DIAGRAM O_n = S_n

SUM SGN +4	S +3	S +2	S +1	S 0	S -1	S -2	S -3	S -4	S -5	S -16	S -17	S -18	S -19	S -20	S -21	S -22
2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²
SGN																

NOTE 2

NOTE 1. When nonaccumulating, all four MSB will indicate the sign of the product. The PR-0 term will also indicate the sign except for the one exceptional case when multiplying -1×-1 . Note that, with the additional significant bits available on this multiplier, -1×-1 is a valid operation yielding a +1 product.

NOTE 2. There is no change in the format whether one is accumulating the sum of products or simply doing single products. However, the three additional most significant bits are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumulation off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position guarantees that the largest number field will be used. In operation the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portion of the accumulator. As an example, when the sum only occupies the least three bit positions then the sign will be extended through the 24 most significant positions.

The latter factor allows one to detect imminent overflow/underflow should this be desired. Using an off-chip exclusive-OR gate connected to the sign and the next most significant bit will flag imminent overflow/underflow. When the two inputs are different, the exclusive-OR gate goes to a logic one state. In this case four more multiply-accumulate cycles would be allowable without overflow/underflow, but a fifth could possibly cause overflow/underflow depending upon the magnitude of the sum steps.

NOTE 3. Format is shown using a 2's complement fractional notation. In this notation the location of the binary point signifying separation of the integer and fractional fields is just after the sign, between the sign and the next most significant bit for the multiplier inputs. This scheme is carried over to the output format, except that an extended significance to the integer field is provided (to extend the utility of the accumulator). Consistent with the input notation the output binary point is located between the PR-0 and PR-1 bit positions (for the nonaccumulate mode). For the accumulate mode the binary point position is the same between the S+0 and S-1 bit positions.

It is arbitrary where the binary point is considered located as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.

3.5.10 Conclusions on Applications of SPAU 2

It was shown in these sections two different approaches to solutions of arithmetic algorithms using SPAU 1 and SPAU 2. It is evident that SPAU 2 is generally superior and manifestly simpler to program. For these reasons, the design during the latter period of this contract concentrated on the SPAU 2 and made debugging iterations on the layout to satisfy all problems and meet specifications. A complete commercial specification is the subject of Appendix C. This specification is listed under TRW house number TDC 1003J.

Packaging of the SPAU 2 changed from the 64 lead flat pack used on SPAU 1 to a heat studded 64 lead DIP. This package arrangement allows the SPAU 2 to operate in still air at a case temperature of 125°C.

Processing yield measured on this 256 by 256 mil chip is approximately 40% at wafer probe test. This corresponds to approximate defect density in processing to 2.5 defects/cm², D_0 . We feel this most complex chip of the set has demonstrated all original goals and was brought to a complete manufacturing state.

The industry should profit from the organizational structure of the SPAU 2. We feel it serves as a model for innovative high speed digital filter applications. One lesson it teaches that goes beyond the hardware accomplishment is that multiplication and accumulation can be considered simultaneous operations rather than disjoint as normally practiced. Also, multiplication and addition are equal weighted operations.

This means that multiplications do not have to be minimized in preference to addition as commonly considered standard practice in the field. The hope is that this new freedom will allow designers to invent more efficient algorithms. Only time and full exploitation of the SPAU 2 concepts will tell.

SECTION IV

SIGNAL PROCESSING DELAY LINE, SPDL, DESIGN

The Signal Processing Delay Line (SPDL) is a grouping of shift registers primarily designed to facilitate address control of an FFT pipeline processor. It also has general purpose application. The logic diagram in Figure 26 shows the organization of this chip. The upper half is a six-bit wide and five-bit long serial shift register with provision for multiplexing to the output either the third or fifth signal. Input multiplexing of either A or B input signals is also provided. The lower half is the same except for output multiplexing of the first and fifth bit signals. All inputs and outputs are TTL compatible and the outputs have tri-state control.

The shift registers are all D type and edge triggered on the leading clock edge. The inputs are level shifted from TTL to CML levels and the registers are implemented using CML circuits. The output circuit includes output multiplexing at CML levels and level shifting back down to TTL.

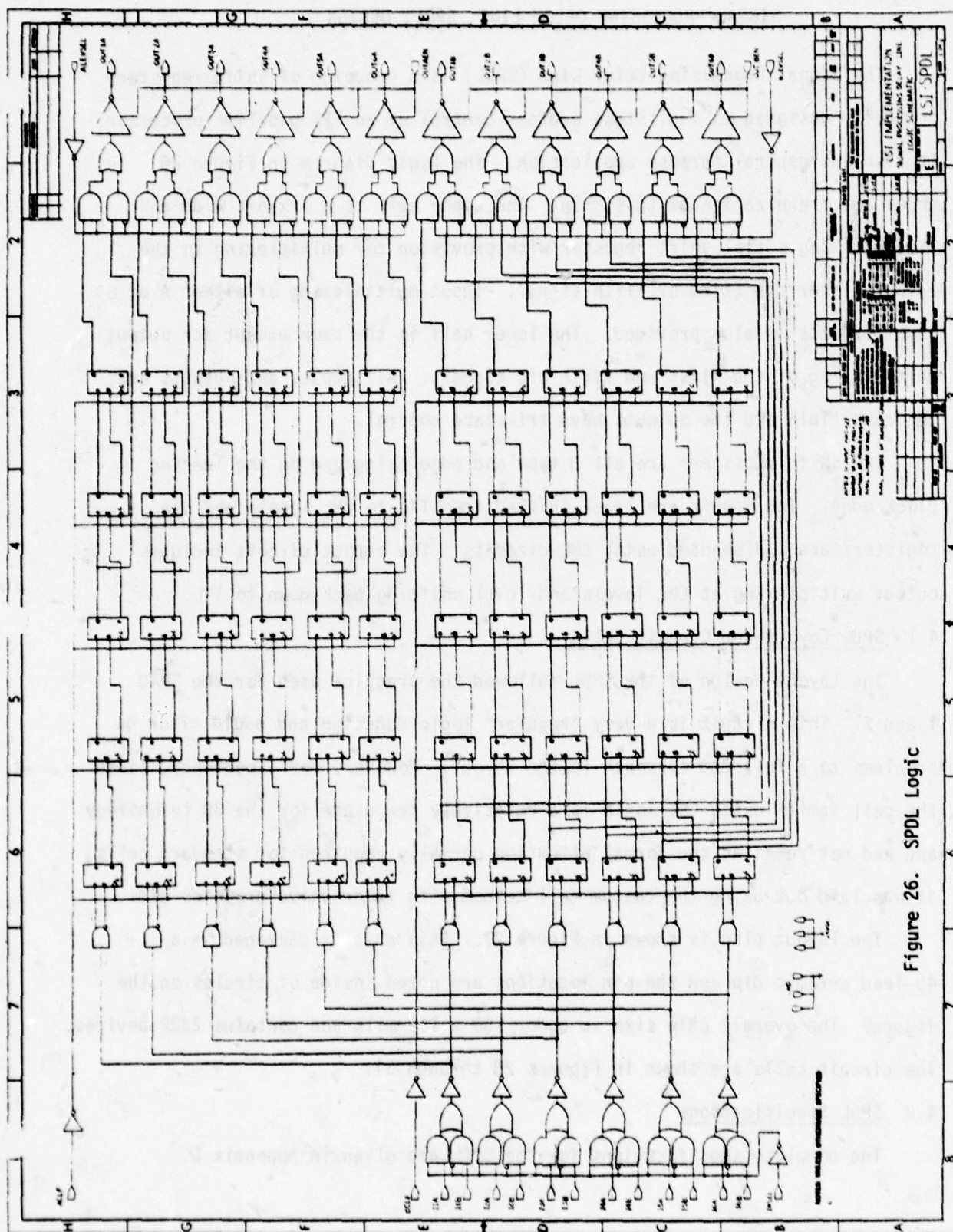
4.1 SPDL Layout and Circuit Cells

The layout design of the SPDL followed the practice used for the SPAU 1 and 2. This circuit is a very "regular" logic function and would offer no problems to a full CAD approach to the layout. However, for expediency, since the cell family using CML logic is a relatively new usage for the 3D technology and had not received the formal attention normally required for standard cells, it was laid out using the custom cell method with interactive graphics aids.

The layout plan is shown in Figure 27. This chip is packaged in a 40-lead ceramic dip and the pin locations are noted inside of circles on the figure. The overall chip size is under 150 x 150 mils and contains 2322 devices. The circuit cells are shown in Figures 28 through 31.

4.2 SPDL Specifications

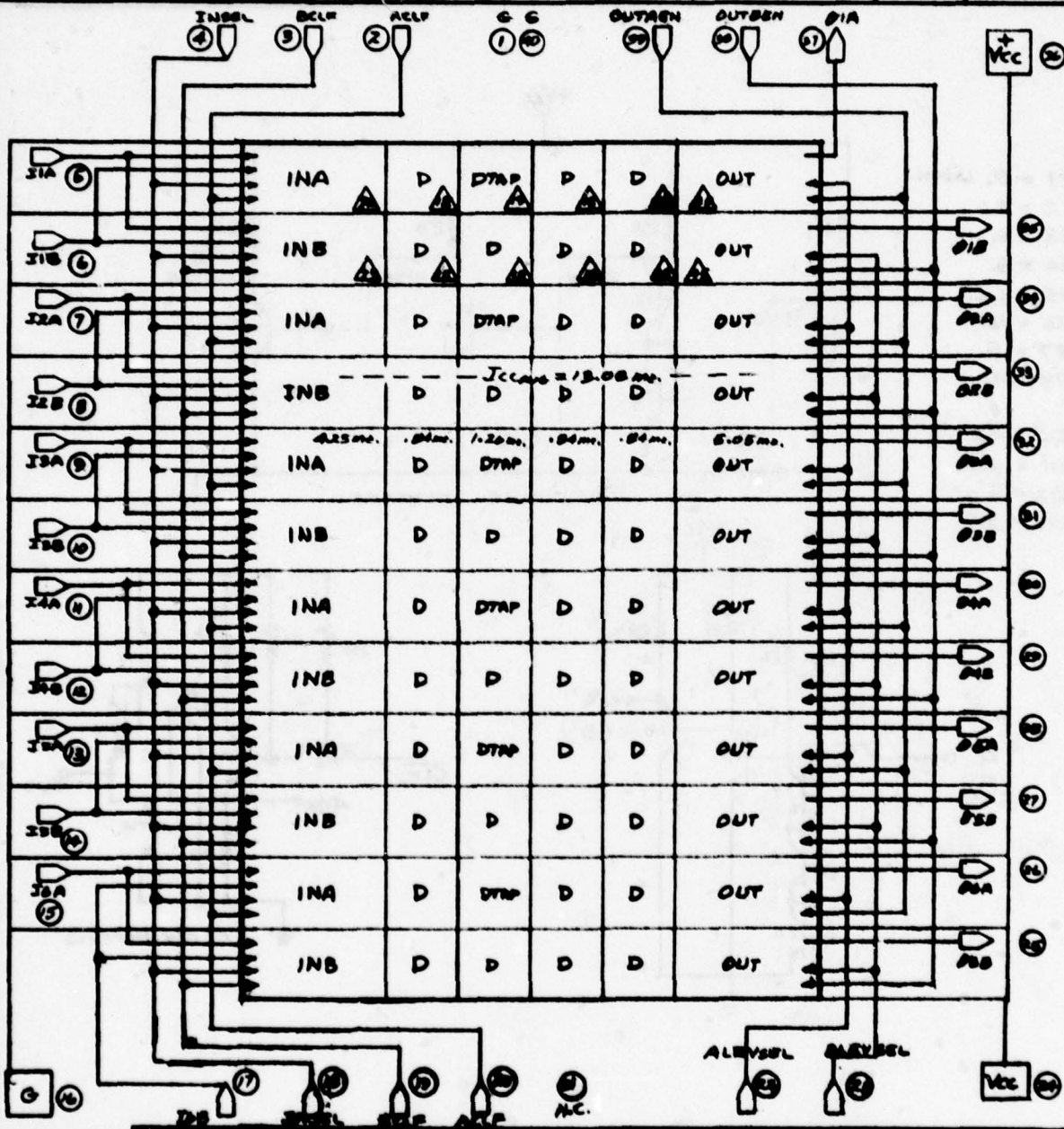
The complete specifications for the SPDL are given in Appendix E.



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SPDL LAYOUT PLAN

SPDL

TOTAL DEVICES 2280

94CMPS/WAVE

CNTL SEL.

CELL AREA

118 X 134 MB

6.8mil/5/1000MJD

Icc = 157 MB

2349-71

SIZE CODE IDENT NO.

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11982

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Figure 27.

SCALE 61

SHEET 1 OF

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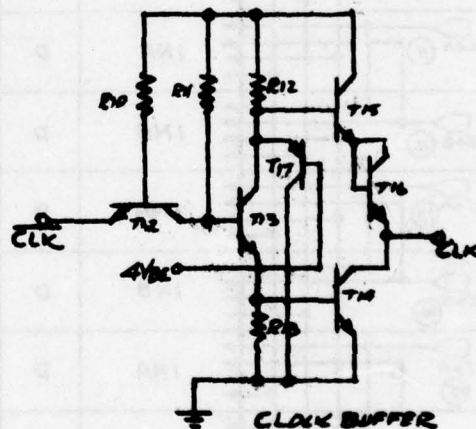
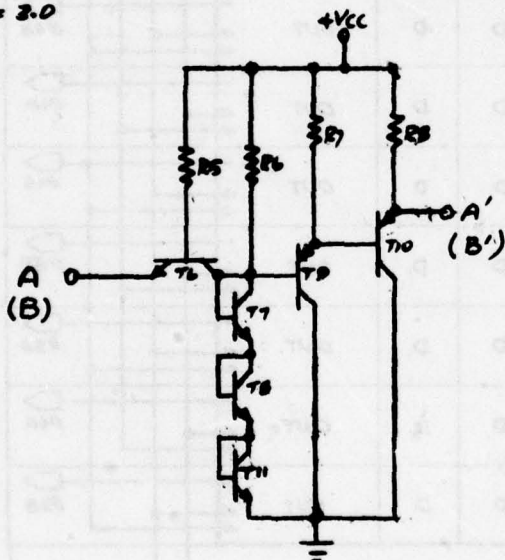
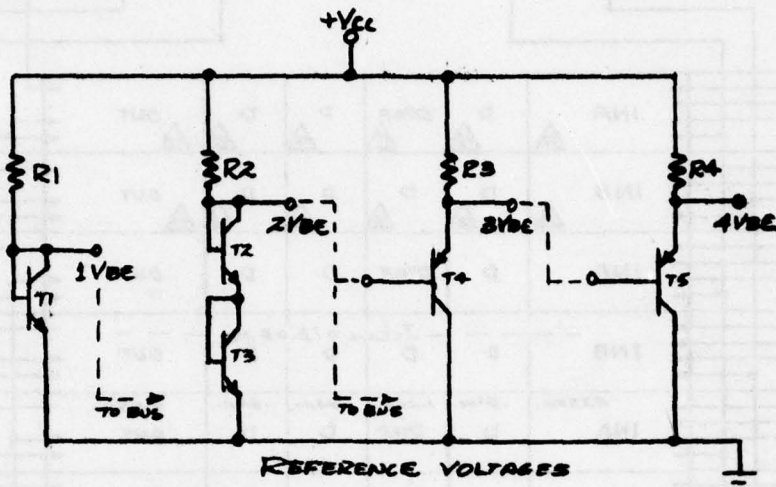
DESCRIPTION

DATE

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$R1 = 9. \text{ LAMPIN.}$
 $R2 = 5.6$
 $R3 = 4.$
 $R4 = 3.$
 $R5 = 60.$
 $R6 = 18.7$
 $R7 = 5.$
 $R8 = 4.$

$R10 = 43.$
 $R11 = 10.1$
 $R12 = 4.0$
 $R13 = 3.0$



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CELLINA (SEE SHEET 2)

SPDL

SIZE

CODE IDENT NO.

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Figure 28.

MJO

2349-71

SCALE

62

SHEET 1 OF 2

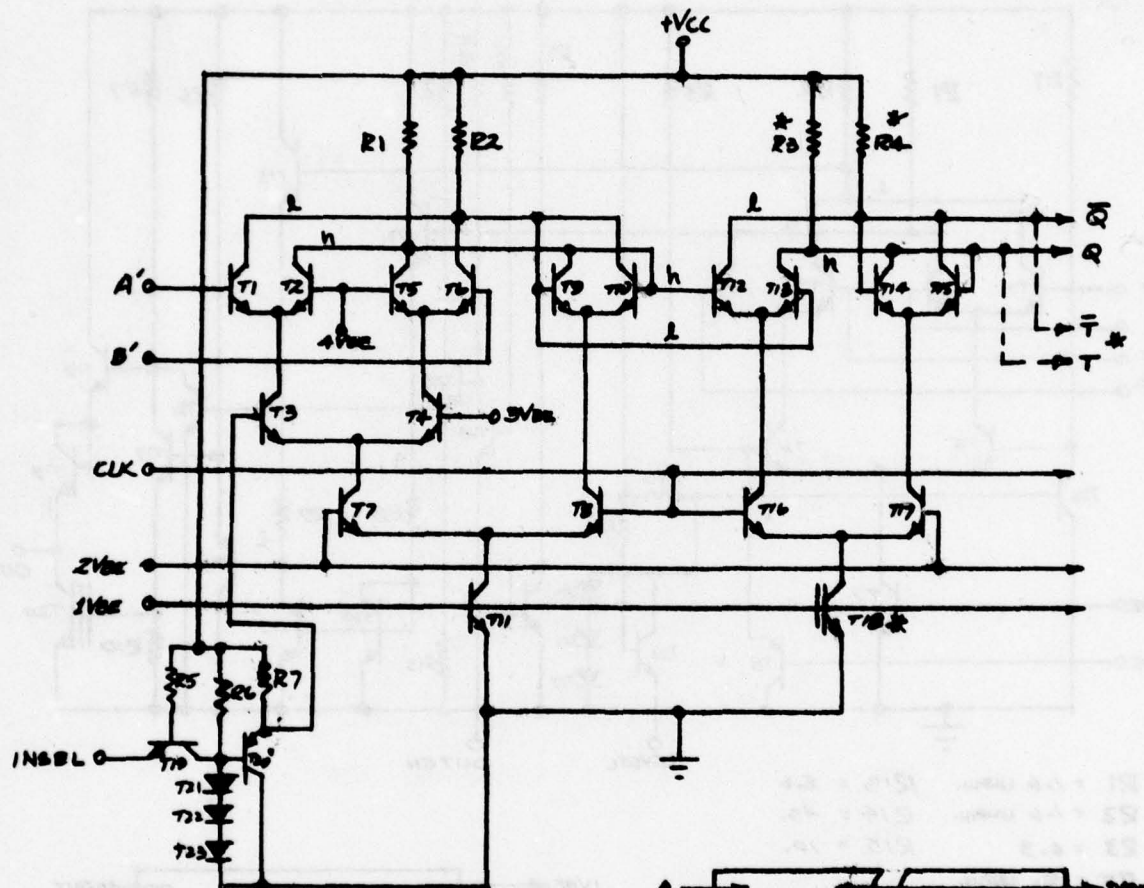
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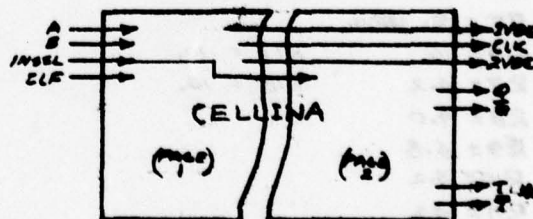
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CELLINA DEVS# = 72

CELLUNB DEVS# = 73



R1 = 1.6 UNPIN. R7 = 7.6
 R2 = 1.6 UNPIN.
 R3 = 1.6 or .8 UNPIN.
 R4 = 1.6 or .8 UNPIN.
 R5 = 45.
 R6 = 11.



* CELLUNB has top outputs T1 through T10. T10 is doubled & T1 through T9 are halved.

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CELLINA (CELLUNB*)

SPDL

SIZE

A

CODE IDENT NO.

11982

SK

Figure 29.

SCALE

63

SHEET OF

SK

REVISIONS

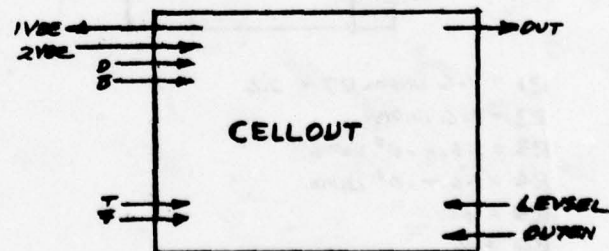
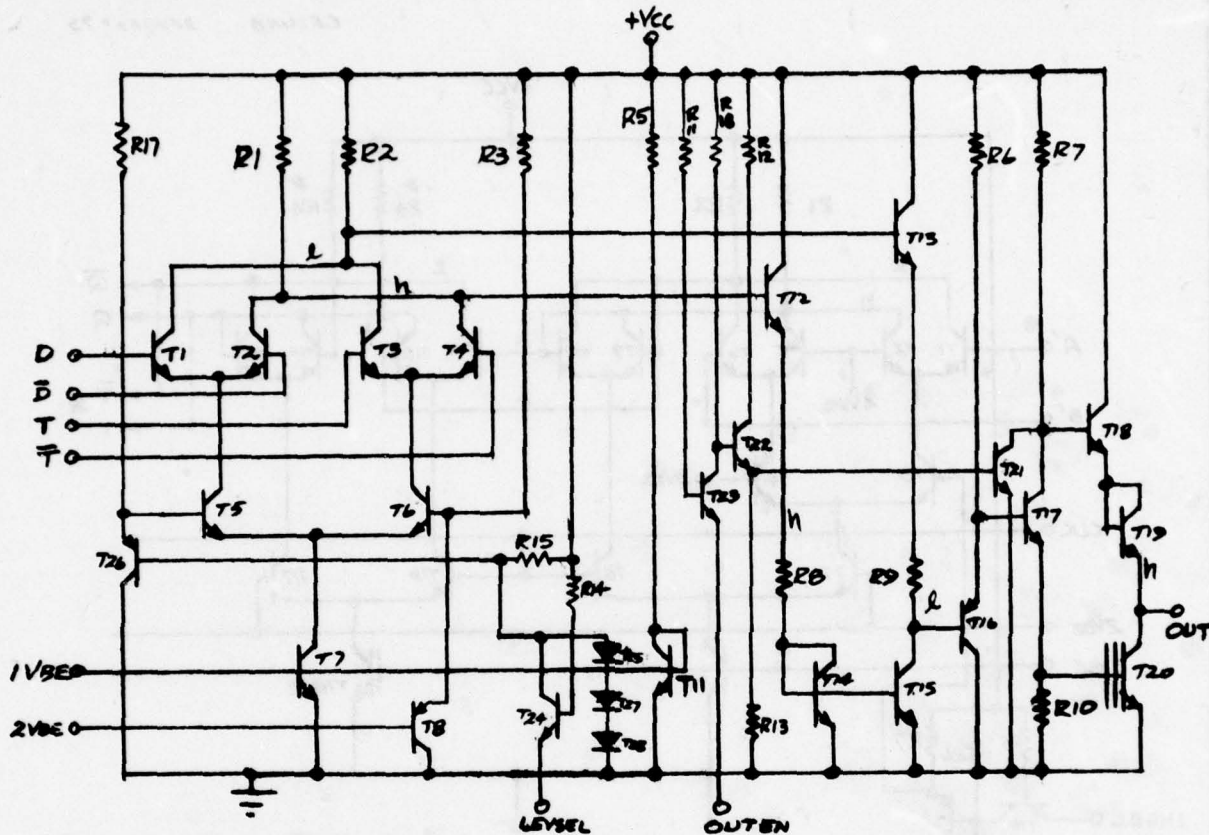
LTR

DESCRIPTION

DATE

APPROVED

DEVICES = 45



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CELLOUT

SPDL

SIZE

CODE IDENT NO.

A

11982

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Figure 30.

SCALE

64

SHEET 1 OF

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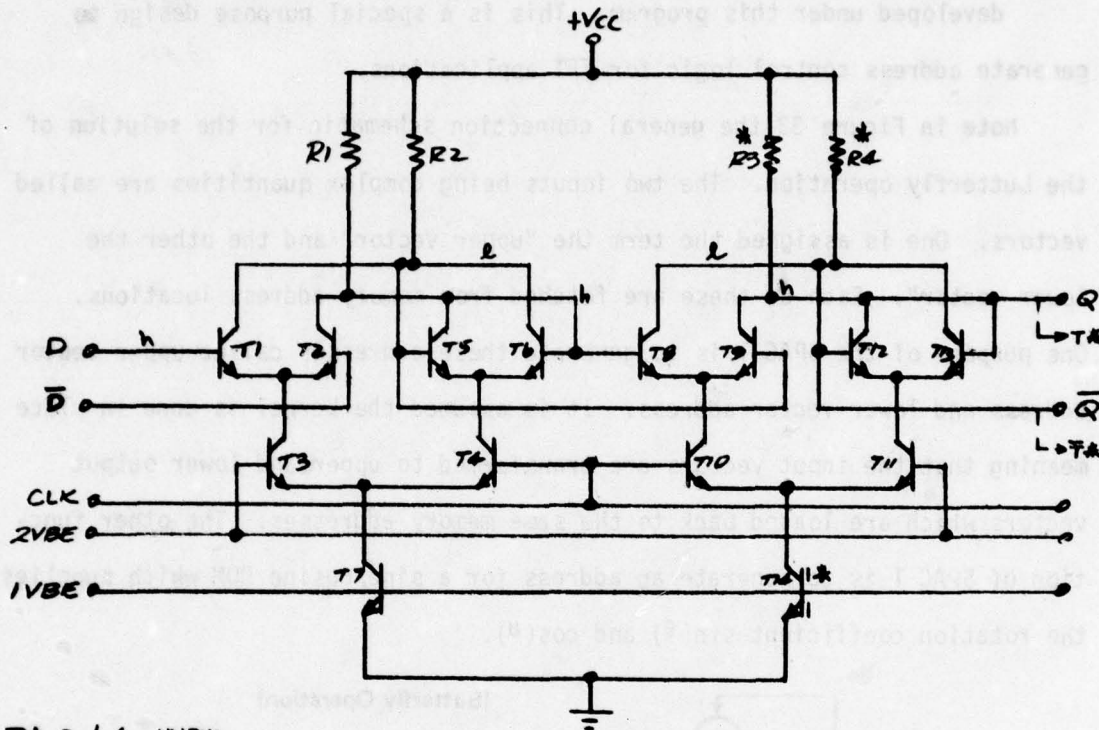
DESCRIPTION

DATE

APPROVED

CELLD
(DTAP)

DEVICES = 18 (10)
POWER = 4.25 mW



R1 = 1.6 UNPIN.

R2 = 1.6 UNPIN.

R3 = 1.6 or .8* UNPIN.

R4 = 1.6 or .8* UNPIN.

* FOR DTAP
HALVE RESISTOR
AND DOUBLE T14



ENGINEERING SKETCH

ORIGINATOR

DATE

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CELLD (CELLDTAP *)

SPDL

SIZE

CODE IDENT NO.

A

11982

SK

Figure 31.

SCALE

65

SHEET 1 OF

SECTION V SPAC-1 DESIGN

The Signal Processing Arithmetic Control (SPAC) is the third type chip developed under this program. This is a special purpose design to generate address control logic for FFT applications.

Note in Figure 32 the general connection schematic for the solution of the butterfly operation. The two inputs being complex quantities are called vectors. One is assigned the term the "upper vector" and the other the "lower vector". Each of these are fetched from memory address locations. One purpose of the SPAC 1 is to generate these addresses called upper vector address and lower vector address. It is assumed the kernel is done in place meaning that the input vectors are transformed to upper and lower output vectors which are loaded back to the same memory addresses. The other function of SPAC 1 is to generate an address for a sine/cosine ROM which supplies the rotation coefficient $\sin(\theta)$ and $\cos(\theta)$.

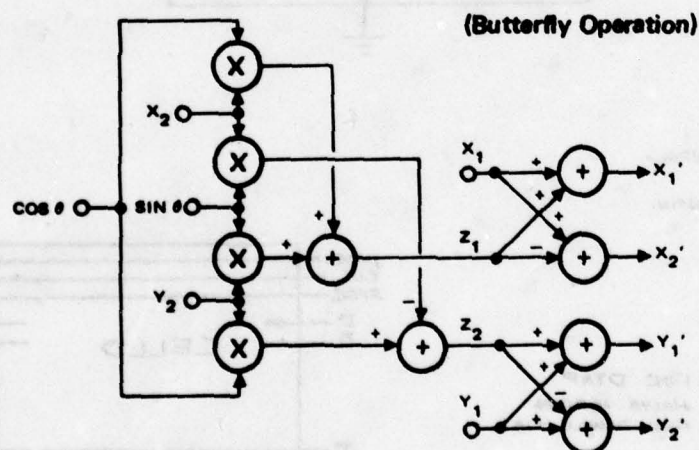


Figure 32. SPAC 1 Outputs

Upper vector address of vector, $x_1 + jy_1$

Lower vector address of vector, $x_2 + jy_2$

Rotation coefficient address of ROM for $\sin(\theta)$ and $\cos(\theta)$

The purpose of the Address Control Logic Chip is to generate all the addresses automatically for any size FFT desired. The size of the FFT is simply loaded into the circuit during the preset cycle, Table 13, and then it outputs a different set of addresses after each clock pulse following the algorithm in Table 14. The addresses generated are the upper vector address to the butterfly, the lower vector address and the rotation coefficient address. The SPAC 1 is implemented in a five-bit slice and requires two chips for a 1024 point FFT. The circuit is designed for a 40-pin flatpack. It requires no control except for a preset for initialization. The circuit normally runs at 1/4 the clock rate of the SPAU 1 butterfly due to the fact that a new set of addresses are generated by each clock, which are then used during four cycles of the SPAU 1. Figure 33 illustrates the FFT Address designations at different times. Each spread is separated into an upper and lower address block from which a "butterfly" is loaded as inputs and to which the results are returned. After the completion of each butterfly operation, the addresses are incremented until the end of the spread or level. The actual sequence of addresses by the LSI are shown in Figure 33. A flow chart (Figure 34) explaining the operation of the hardware, follows. The block diagram of the SPAC 1 logic is shown in Figure 35. The block diagram in Figure 36 is the same except that logic is arranged into five-bit cells.

The SPAC 1 design was completed through the simulation and layout stage, but not masked or fabricated. This was a custom design with 3500 devices and a chip size of 226 x 218 mils. Due to the extensive feedback in the counter logic the chip was less efficient than found in the other custom designs. Experience with logic of this sort found in SPAC 1 teaches that considerable rework is often necessary to completely debug the chip. For these reasons, a simpler chip using a computer automated approach was selected for meeting these requirements. This was the reason for completing the hardware delivery using the SPAC 2 design taken up in the next section.

5.1 SPAC 1 Specification and LSI Details

These are shown in Appendix F.

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TABLE 13.

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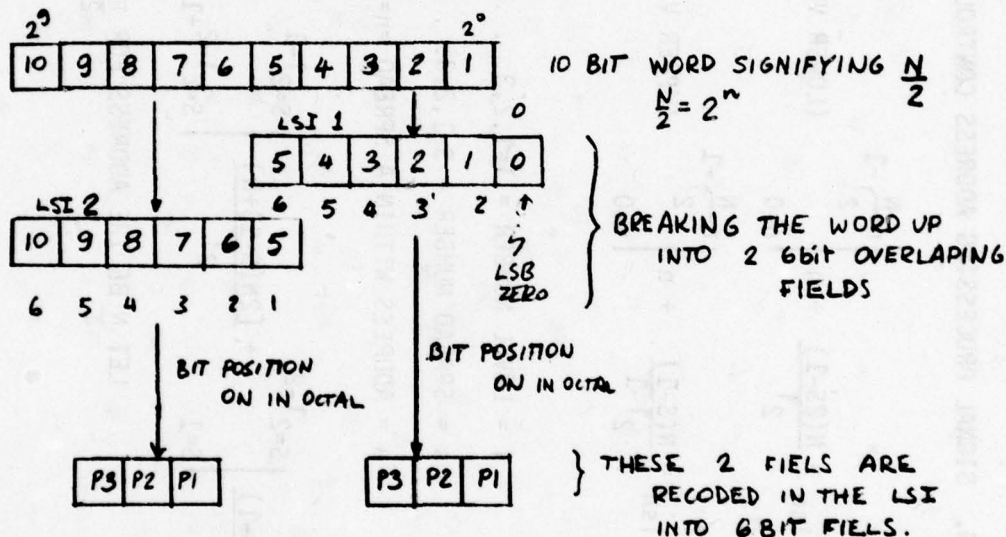
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THE PROGRAM CODE ENTERS THE FFT POINT SIZE (N) AS $N/2$ IN THE FOLLOWING FORMAT.

- 0 ALL BITS IN THE 5 BIT SLICE ARE ZERO, INCLUDING THE MOST SIGNIFICANT BIT OF THE LOWER ORDER SLICE.
- 1 THE MSB OF THE NEXT LOWER ORDER SLICE IS A ONE.
- 2 1ST BIT OF THE 5 BIT SLICE
- 3 2ND BIT OF THE 5 BIT SLICE
- 4 3RD BIT OF THE 5 BIT SLICE
- 5 4TH BIT OF THE 5 BIT SLICE
- 6 5TH BIT OF THE 5 BIT SLICE



EXAMPLE: IF $\frac{N}{2} = 2^9 = 10000/00000$
 1024 PT FFT
 $N/2 = 512 = 2^9$

Diagram illustrating the bit positions in octal for the example. The bit positions are 6, 5, 4, 3, 2, 1. The bit positions in octal are labeled "BIT POSITION ON IN OCTAL".

THE PROGRAM CODE BECOMES:
 $6, 0_8$ for 2 LSI's

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LSI ADDRESS CONTROL
PROGRAMMING CODE

SIZE

A

CODE IDENT NO.

11982

SK

SCALE 69

SHEET 1 OF 3

TABLE 14. SIGNAL PROCESSING ADDRESS CONTROL LSI FUNCTIONS

$$L_{1sn} = \frac{N(2S-1)}{2} + n \quad \left| \begin{array}{l} n = \frac{N}{2} - 1 \\ n = 0 \end{array} \right. \quad (\text{LOWER VECTOR ADDRESS})$$

$$U_{1sn} = \frac{N(S-1)}{2^{1-1}} + n \quad \left| \begin{array}{l} n = \frac{N}{2} - 1 \\ n = 0 \end{array} \right. \quad (\text{UPPER VECTOR ADDRESS})$$

1 = LEVEL NUMBER = 1, 2, 3, . . . $\log_2 N$

s = SPREAD NUMBER = $S=1, 2, 3, . . . 2^{1-1}$

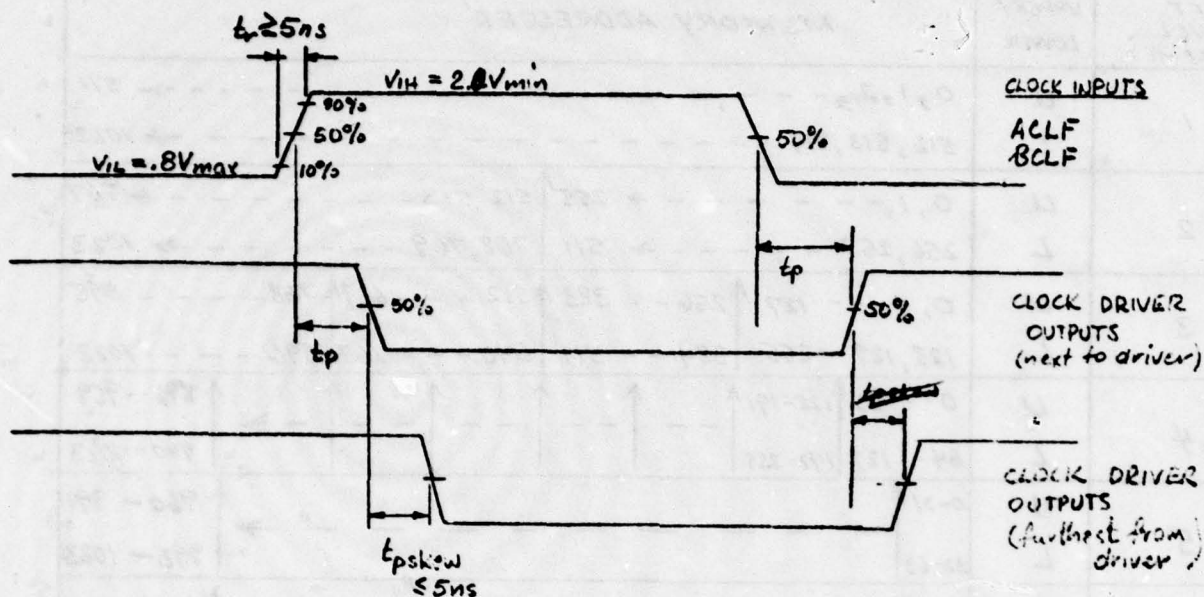
n = ADDRESS WITHIN A SPREAD = $n=0, 1, 2, . . . (\frac{N}{2} - 1)$

$$C_{1s} = \frac{2N(S-1)}{2} \quad \left| \begin{array}{l} S=2^{1-2} \\ S=1 \end{array} \right. + \frac{[2N(S-1)+N]}{2} \quad \left| \begin{array}{l} S=2^{1-1} \\ S=2^{1-2}+1 \end{array} \right. \quad (\text{COEFFICIENT ADDRESS})$$

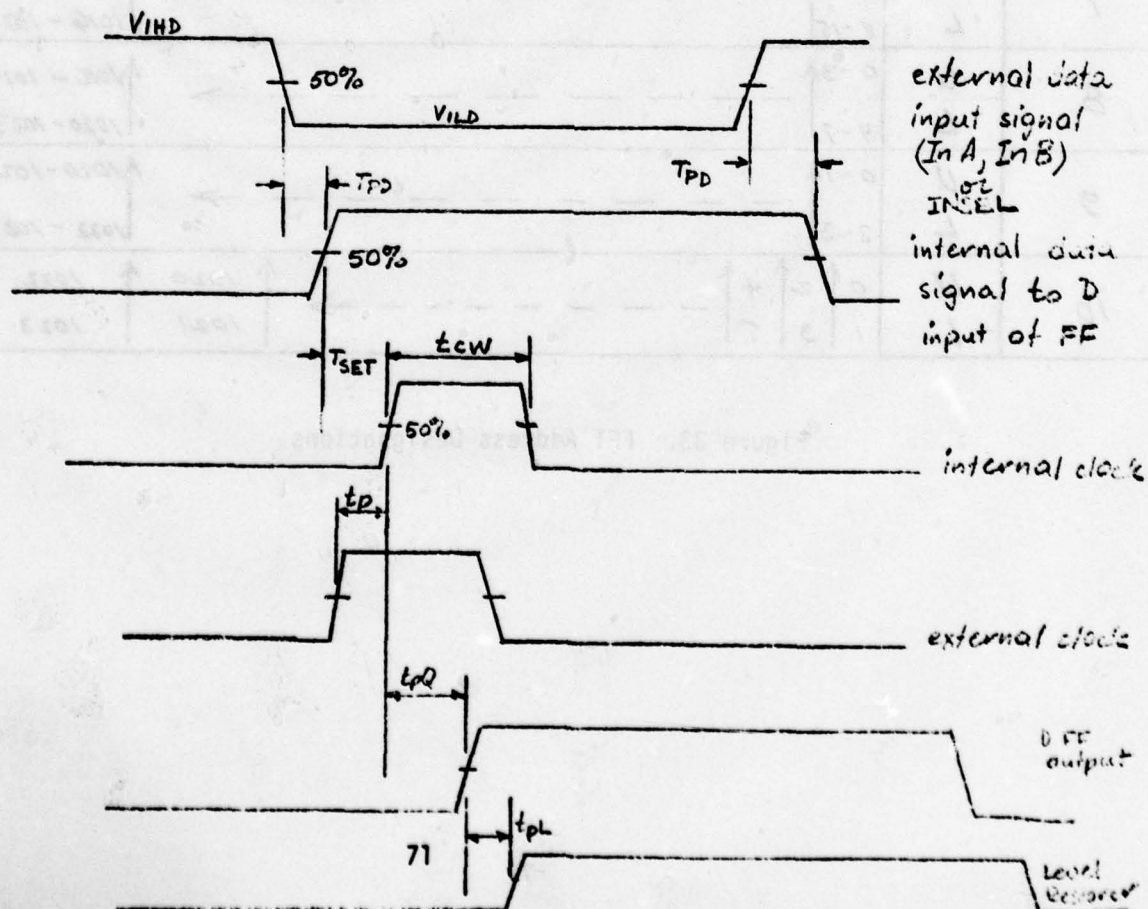
LET $\frac{N}{4}$ BE THE ADDRESS FOR $\frac{\pi}{2}$

CLOCK DRIVER

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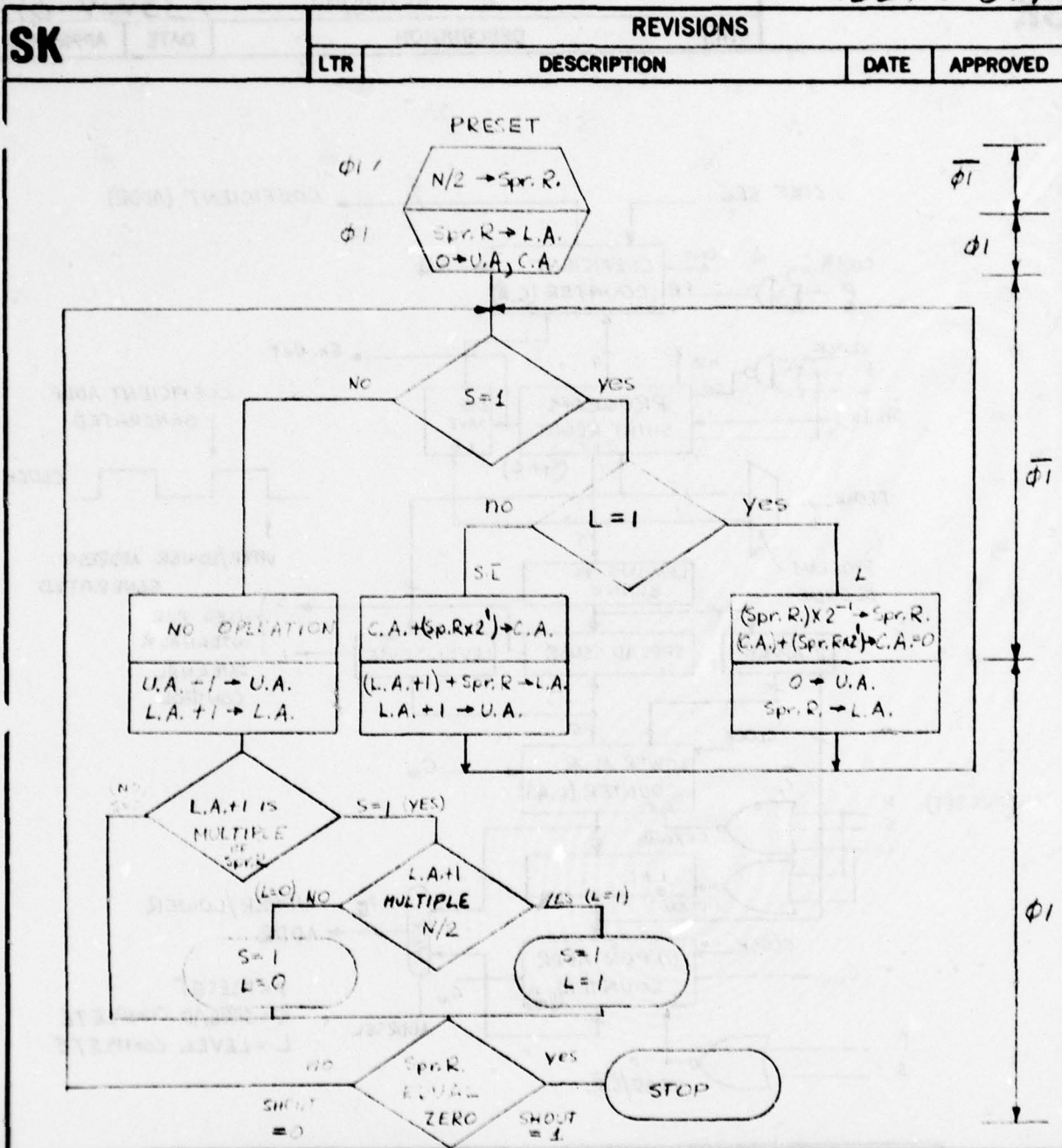
D FLIP FLOP



FFT LEVEL (FRAME)	UPPER / LOWER	MEMORY ADDRESSES
1	U L	0, 1, 2, ... → 511 512, 513, 514 ... → 1023
2	U L	0, 1, ... → 255 512, 513 ... → 767 256, 257 ... → 511 768, 769 ... → 1023
3	U L	0, 1 ... 127 256 ... 383 512 ... 639 768 ... 895 128, 129 ... 255 384 ... 511 640 ... 767 896 ... 1023
4	U L	0 ... 63 128-191 896 ... 959 64 ... 127 192-255 960 ... 1023
5	U L	0-31 960-991 32-63 992-1023
6	U L	0-15 992-1007 16-31 1008-1023
7	U L	0-7 1008-1015 8-15 1016-1023
8	U L	0-3 1016-1019 4-7 1020-1023
9	U L	0-1 1020-1021 2-3 1022-1023
10	U L	0 2 4 ... 1020 1022 1 3 5 ... 1021 1023

Figure 33. FFT Address Designations

7334.4-097



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ORIGINATOR <i>Alfred J. Hamon</i>	DATE	Figure 34. FFT ADDRESS CONTROL ALGORITHM	
SIZE A	CODE IDENT NO. 11982	SK	
SCALE 73	SHEET 1 OF		

SK

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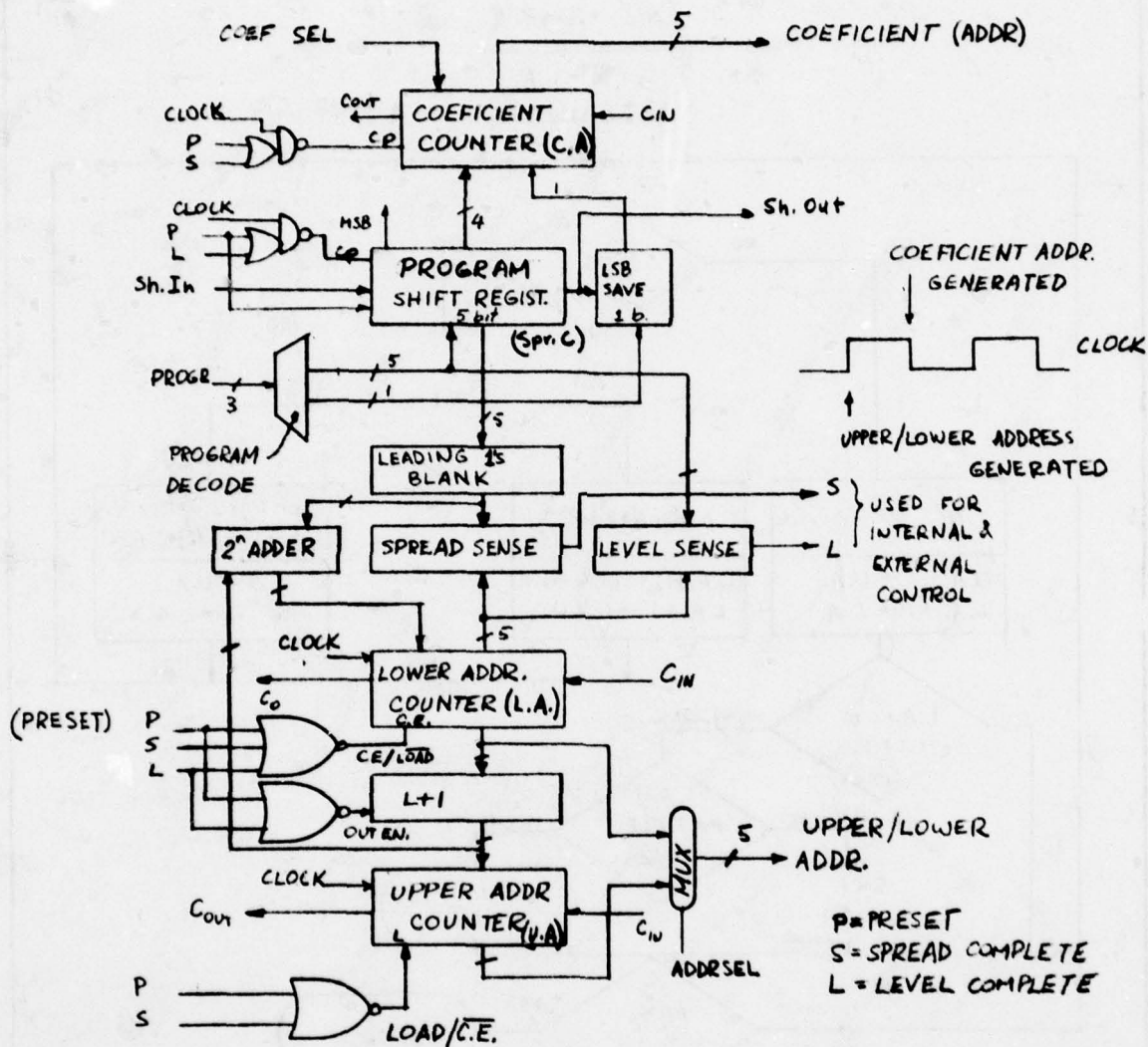
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Figure 35.

ADDRESS CONTROL LOGIC

SIZE

A

CODE IDENT NO.

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LSI-ACB-B

SCALE

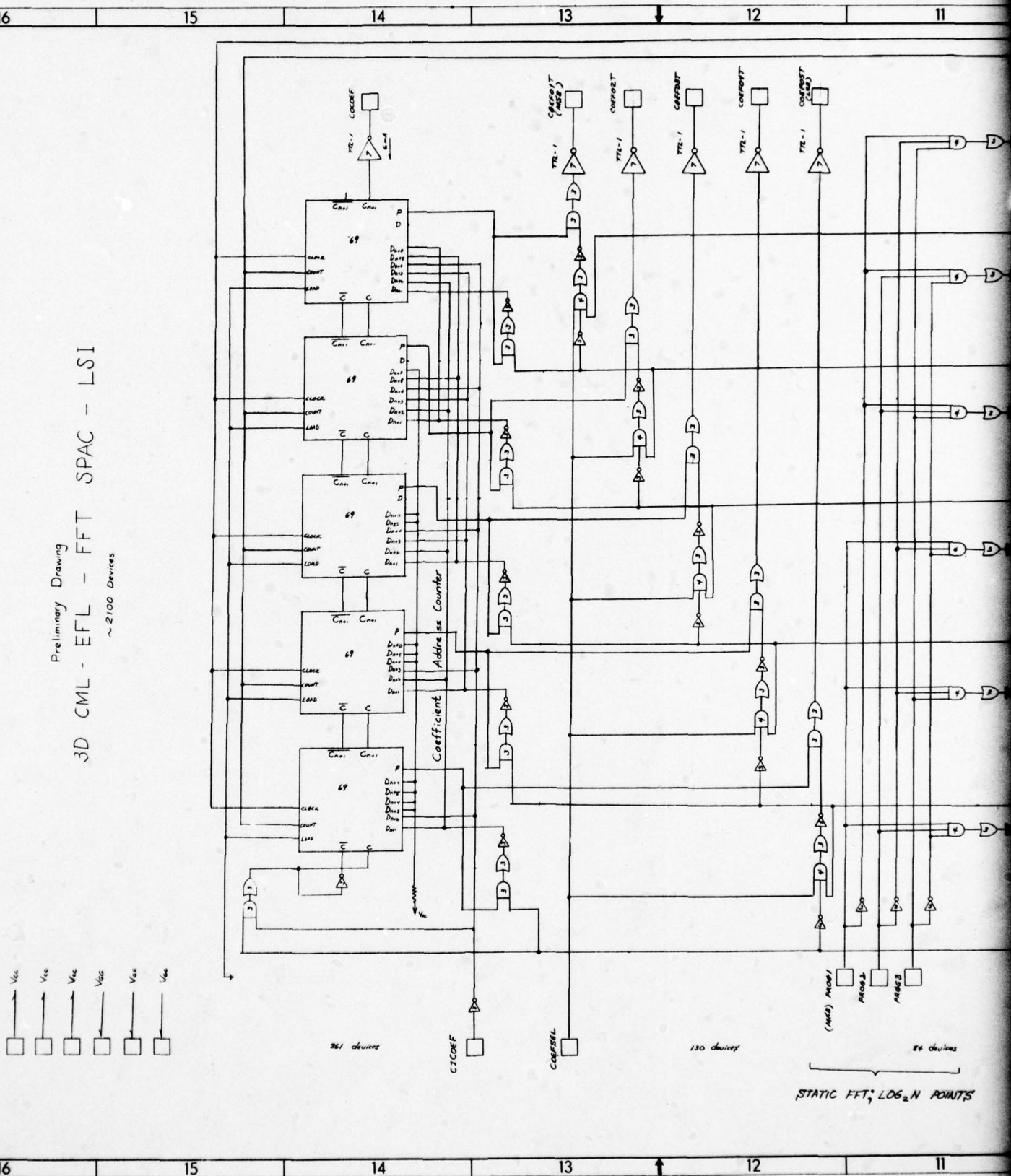
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SHEET 1 OF

SYSTEMS 823 REV. 12-71

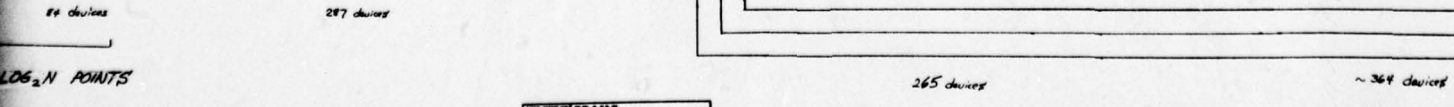
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3D CML - EFL - FFT SPAC - LSI
Preliminary Drawing
~2100 Devices



11	10	9	8	7	6
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Cms. GARDNER JR.



5.2 SPAC 2, Design

Hardware deliveries were completed using a simplified alternative to the custom design SPAC 1 chip. This design is called SPAC 2 and it is made from a universal array LSI, TRW's Configurable Gate Array, CGA. This design has the following features:

- a. Brings another LSI technique, the gate array approach, to the LSI Implementation program.
- b. Offers a flexible approach for application changes where different algorithms for address generation in FFT's may be desired such as frequency to time transformations.

A block diagram of a complete FFT address generator using the SPAC 2 is shown in Figure 37. Each SPAC 2 incorporated a five-bit address slice, 32-point FFT. Using two chips provides a 10-bit slice for 1024 point FFT. In addition to the SPAC 2 chips other MSI chips for adders and counters, approximately 16 additional chips are required. Using an all MSI approach, approximately 50 chips are required, so the reduced package count saving is quite good.

The SPAC 2 is a controller to other logic as shown in Figure 37. The design of SPAC 2 is based on shift register logic of a type similar to that used in the SPAC 1. The logic diagram for SPAC 2 is shown in Figure 39. The similarity can be seen by comparing this to a row logic section of Figure 5.5.

Figure 38 shows a block diagram for the SPAC 2. A one-bit register element for the coefficient is shown in Figure 40, and the corresponding vector address is shown in Figure 41. There are approximately 26 gates used per bit slice for a five bit slice of 129 gates. This fits well into the 158 gate complement and 40-lead package normally used for the CGA approach. The gate placement and wiring diagram for the SPAC 2 CGA chip is shown in

Figure 42. This drawing is outputted from the CGA approach and is used to check the interconnections. There is one to one correspondence with this and the logic diagram shown in Figure 42. Gate numbers and pad numbers are the same in both drawings.

Appendix G is a summary of the gate specifications and the design information of TRW's Configurable Gate Array.

SK

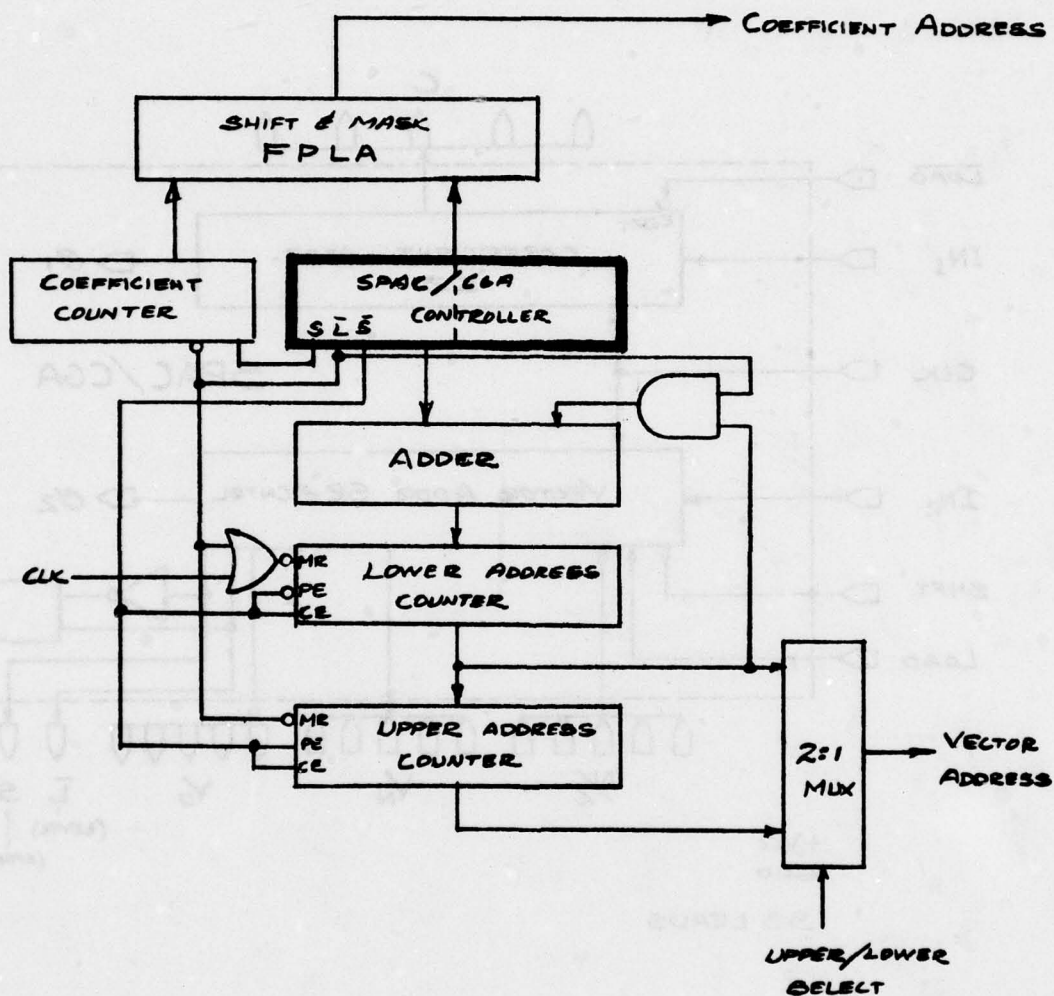
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A. HAMORI

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CL. J. B. B.

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ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

FFT ADDRESS GENERATOR

USING SPAC/CCA APPROACH

SIZE

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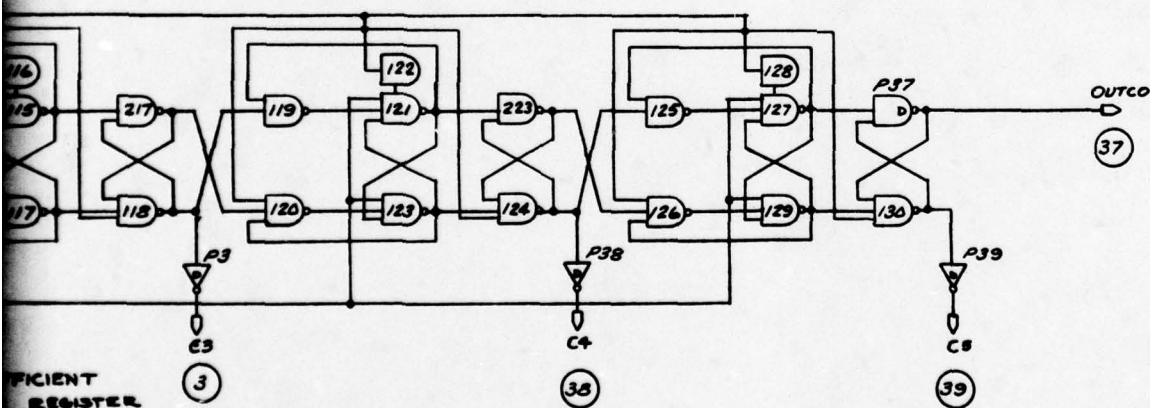
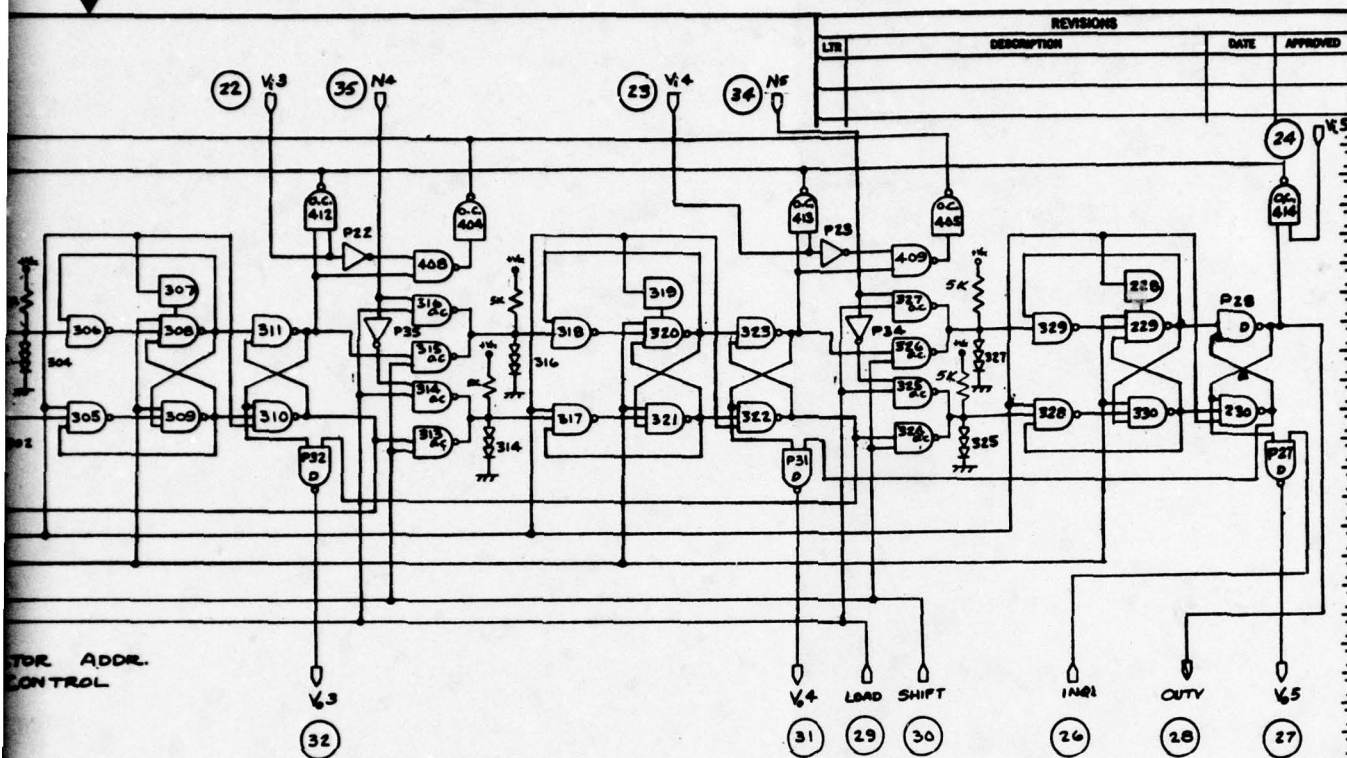
Figure 37.

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SHEET 1 OF

SYSTEMS 523 REV. 12-71



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THE FOLLOWING EQ'S HAVE BEEN ATTACHED TO THIS PRINT TRW ONE SPACE PARK • REDWOOD BEACH, CALIFORNIA SPAC/CGA FFT ADDRESS CONTROL						
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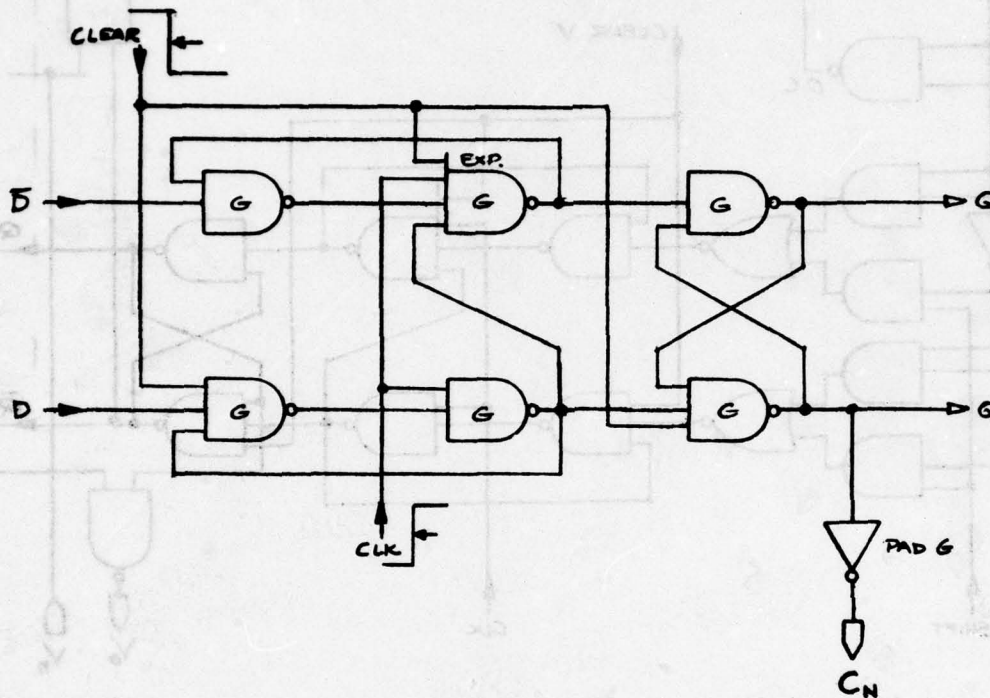
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8 CGA GATE EQUIV.

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TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

COEFFICIENT SR CELL (CGA)
SPAC/CGA

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Figure 40.

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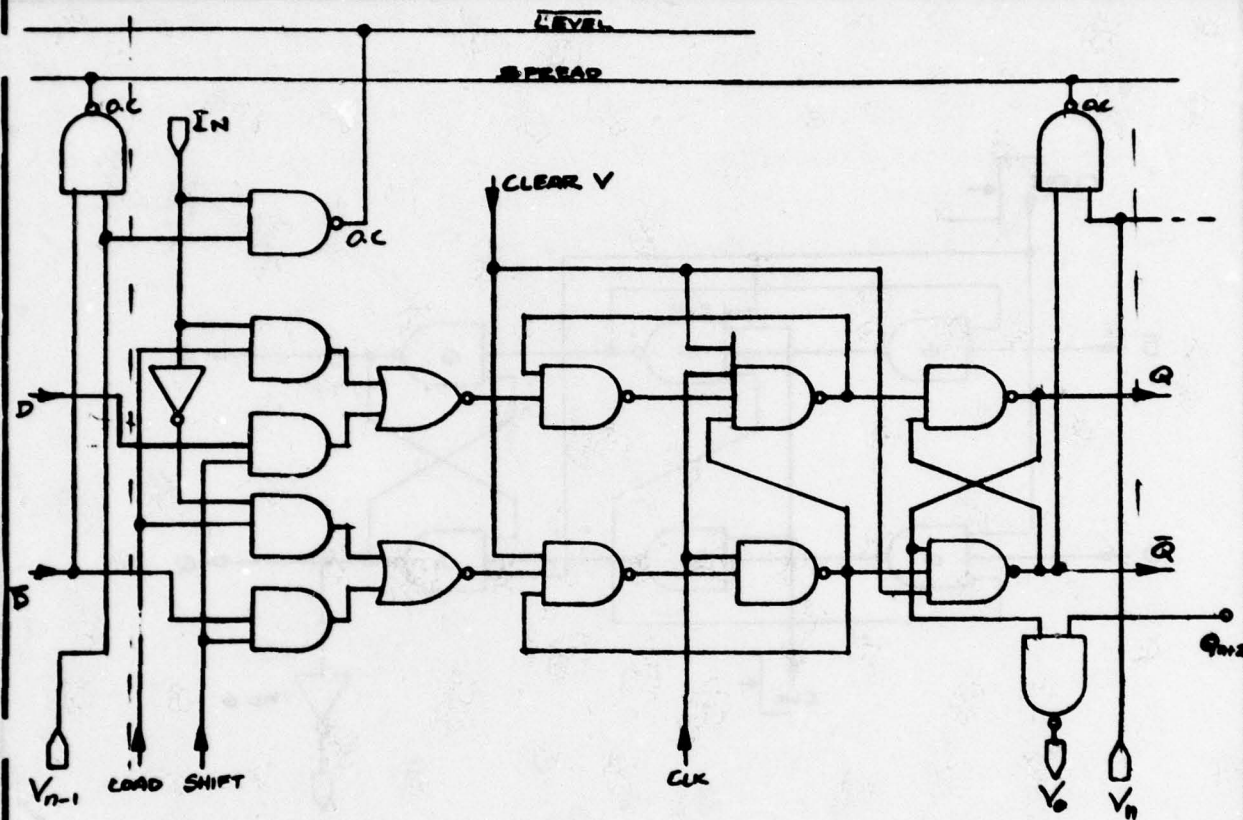
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SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

VECTOR ADDR. CONTROL SR
SPAC/CGA

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Figure 41.

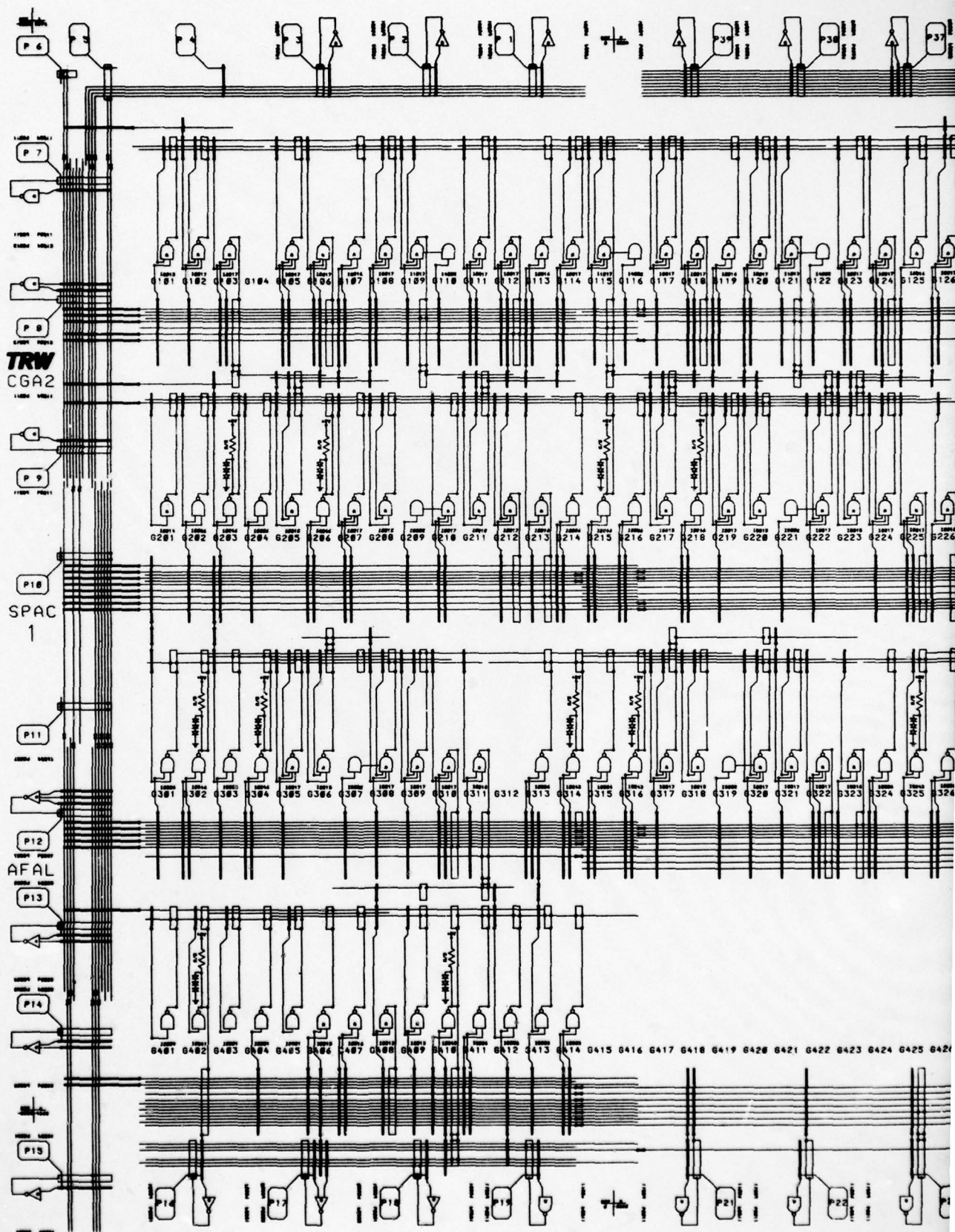
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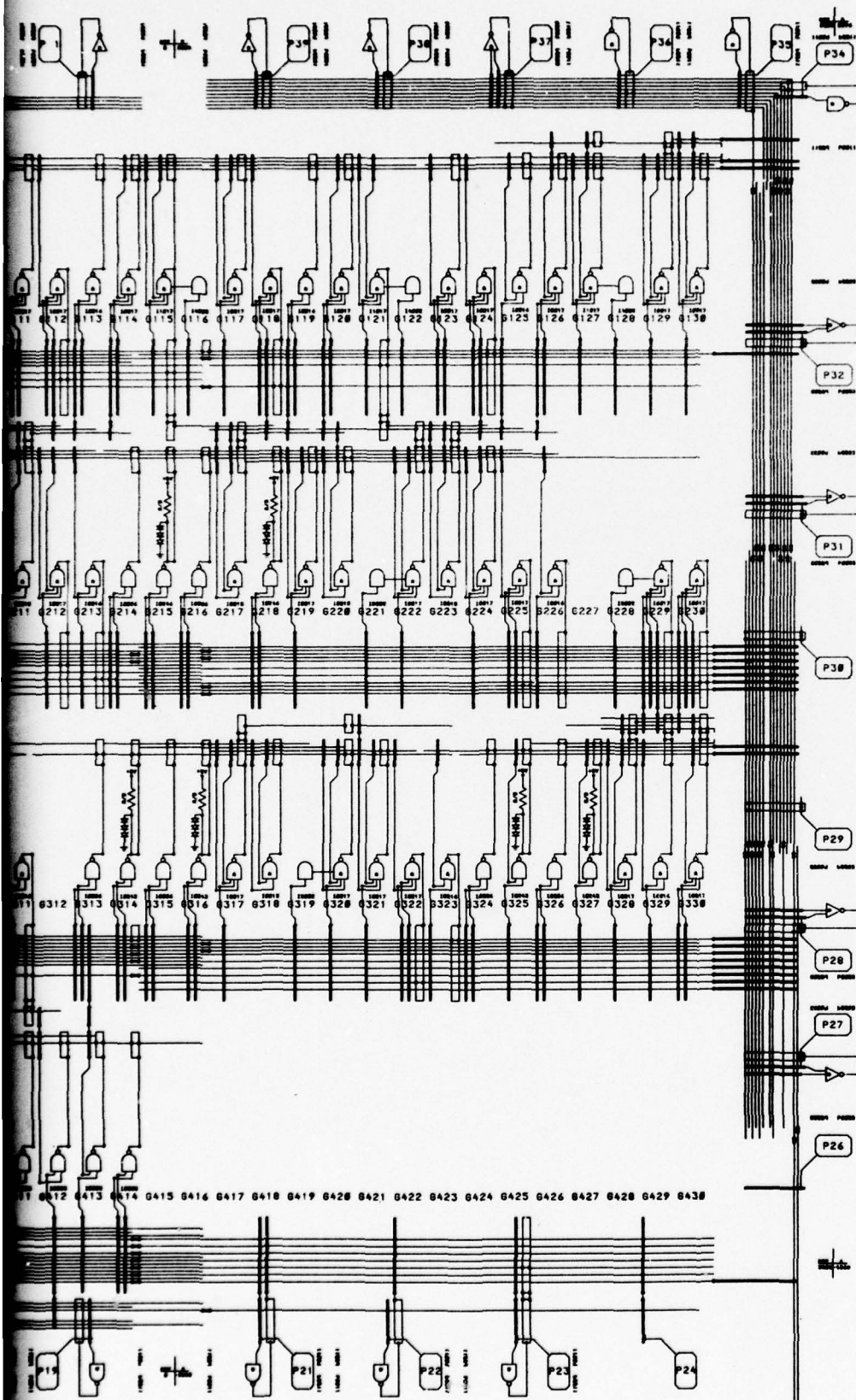


Figure 42. SPAC 2 Gate Check Drawing

SECTION VI LSI/VLSI TECHNOLOGY

The technology used through this study and used to design, fabricate, and deliver packaged chips under this program is the triple diffusion, 3D, technology. This was used for the custom designs as well as the universal array design. Table 15 lists the type and kind of LSI chip along with size, number of devices, and device packing density for all chips delivered under this program.

TABLE 15. SALIENT FEATURES OF LSI CHIPS

TYPE	DESIGNATION	CHIP SIZE mils x mils	NO. OF DEVICES	AREA/DEVICE mils ² /device
Custom Random Logic	SPAC 1	226 x 218	3500	14.1
Custom Uniform Logic	SPAU 1	351 x 315	15,000	7.4
Custom Uniform Matrix Logic	SPAU 2*	256 x 256	13,000	5.1
Custom Uniform Matrix Logic	MPY 16*	278 x 278	18,000	4.3
Custom Uniform Linear Array	SPDL	115 x 134	2,280	6.8
Configurable Gate Array	SPAC 2	208 x 208	1,160	37.3

*Uses reduced geometry

Reviewing Table 15, the most densely packed designs are the uniform matrix or linear type arrays. Most of the chips use 4 micron space and feature dimensions, but SPAU 2 and MPY 16 use 3 micron dimensions and this accounts for the better packing density. The smaller chips suffer from this type of calculation because the total chip area from scribe line to scribe line is taken. For smaller chips more area is used in the curf for pads and things.

The SPAU 1 although listed as unifrom has a good deal of control logic. If this were made with reduced geometry compared with SPAU 2 the device density would be approximately the same, 5.5 versus 5.1 mils²/device compared to the SPAU 2.

6.1 3D-LSI Description

The triple diffusion (3D) bipolar integrated circuit technology was introduced in the early 1960's to meet the impending need for device integration on a monolithic silicon chip.^{1, 2} It offered the most direct and simplest means of producing electrically isolated transistors and resistors on a chip. This remains true today. With this technology, NPN transistors and resistors are self-isolated by PN junctions. PNP's are vertical devices with collectors common with the substrate. The resistors are N type, either collector or collector-pinched. With the advent of LSI, the 3D technology was revived to implement medium speed, typically 5 to 30 MHz, high complexity chips with 2,000 to 20,000 devices. A large number of LSI designs have been produced with sizes ranging from 100 x 100 mils upward.

The reason for using 3D instead of the more prevalent epitaxial method lies in the higher producibility and device density obtainable. Although present 3D practice produces devices with lower alpha cutoff frequencies than epitaxy devices, this has not resulted in a particular handicap for medium speed applications.

The circuit performance within an LSI depends upon optimization of the circuit, given the device characteristics derived from the physical structure. The other way around would be to tailor the process to meet the circuit. Considering the wide versatility of circuit engineering compared to what can be done in a practical manner with physical processes, it seems wiser to tailor the circuit. This has been the course followed, which has led to not-so-conventional circuits that better use the 3D device properties. Several types of these are discussed.

LSI systems employ MSI and SSI in addition to the basic LSI devices. Custom 3D-LSI chips seldom stand alone, but must electrically interface with LSI/MSI/SSI chips in order to achieve cost effectiveness. As a result, two different criteria are adopted, one for the internal logic and the other for the input/output interface.

6.2 Triple Diffusion Process

Since there may be a confusion of names concerned with technologies of similar types, we define the triple diffusion process to mean a process for bipolar

transistors of both types (NPN and PNP) and self-isolated resistors. This process consists solely of an impurity deposition and distribution taken three times in sequence (or by fewer steps using advanced processing means). Figure 43 shows the plan and cross-sectional view of present triple diffused devices.

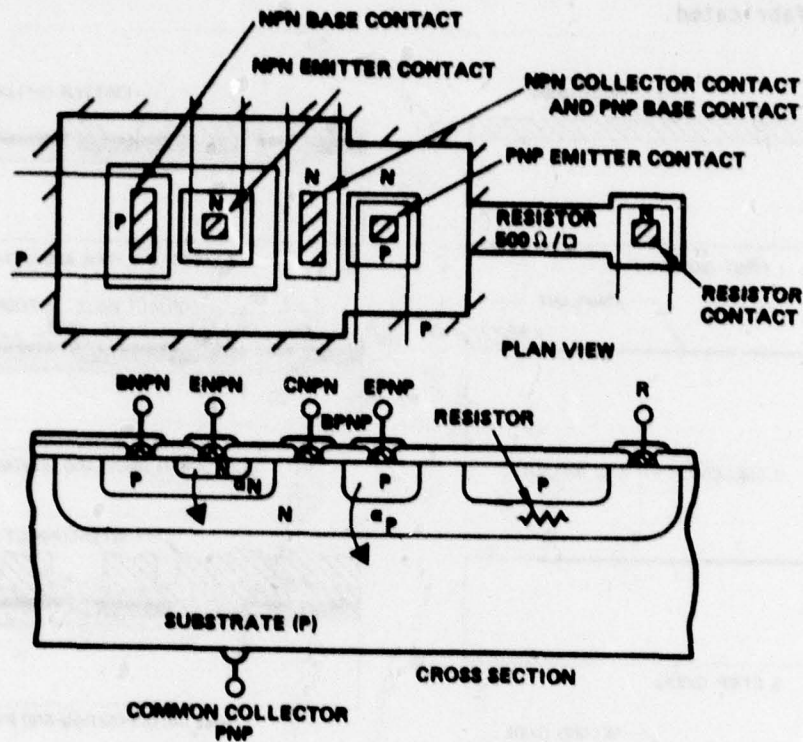


Figure 43. Triple Diffusion Structure

The silicon-substrate is prepared by oxidation, followed by conventional photo-resist mask and etching steps to delineate the "collector" areas. Impurity doping is done by phosphorous ion implantation, followed by a thermal distribution diffusion. The base and emitter regions follow in sequence and are prepared in a similar way. Intraconnections are made by etching electrode contacts through the protecting oxide and depositing Ti-Al metal. Finally, the metal is etched, and the surface is covered with a passivating surface oxide.

Figure 43 shows a PNP transistor coalesced or merged into the NPN transistor. Also, the resistor terminates on the collector of the assembly and is, in fact, a simple extension of the collector region. This property of coalescing structures having a common potential in a circuit reduces the intraconnection complexity and does much to enhance the device density obtainable with 3D.

Figure 44 is a more detailed transistor cross-section showing the principal steps in the process. Also, the N^+ top collector contact ring is shown. This is necessary in order to keep the collector spreading resistance low. Guard-ring construction is used. This is shown as an outer P^+ diffusion around the device; actually, the entire field is P^+ , except for cutouts where transistors or other devices are fabricated.

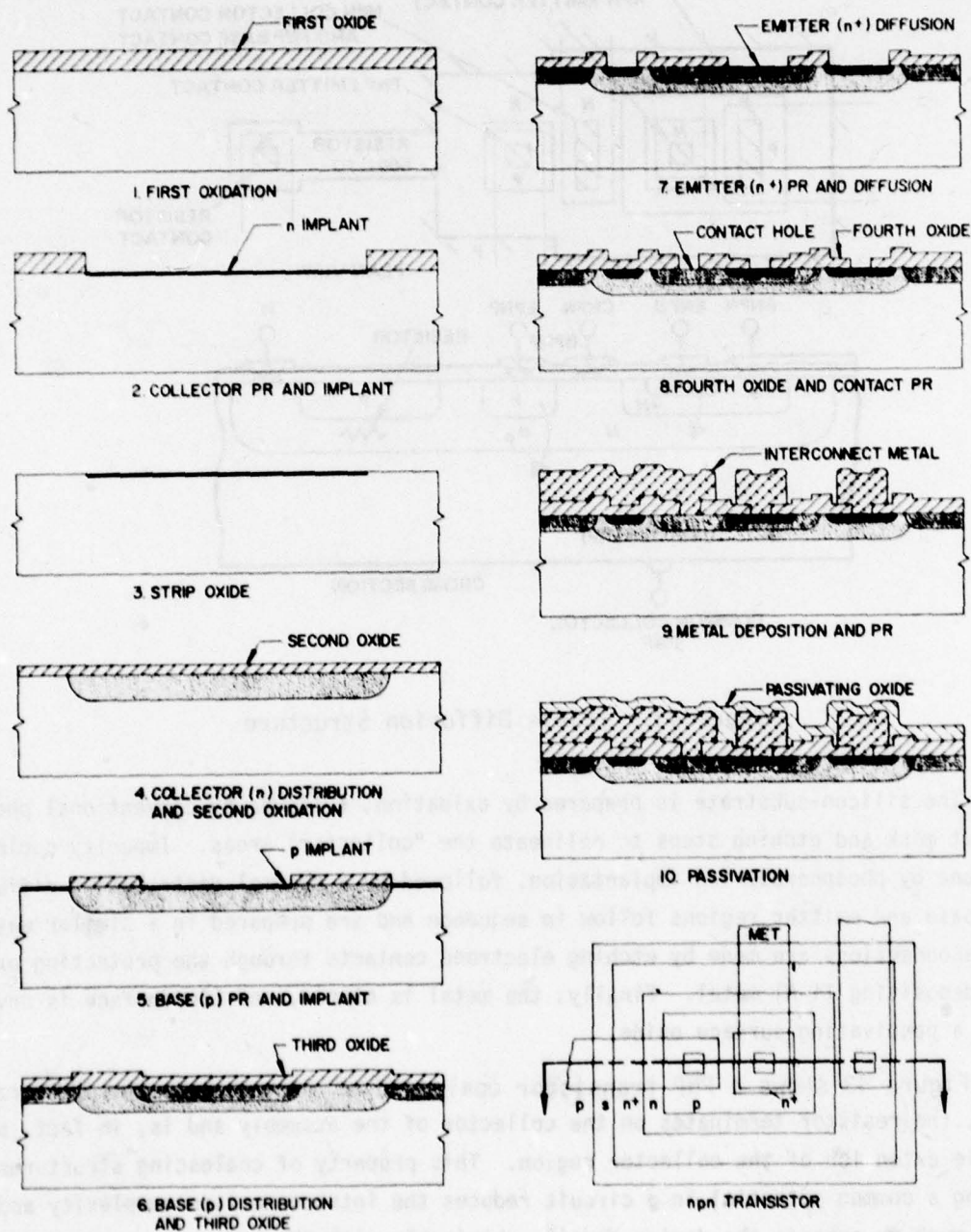


Figure 44. Triple Diffusion Process

6.3 3D DEVICE PROPERTIES

The 3D process uses P type silicon substrate as an active device region as opposed to the weak interaction mode normally processed into IC's. Consequently, the transistor parameters must include this additional effect. PNP's are formed from the P+ "base," N "collector," and P substrate as shown in Figure 45. These are vertical operating devices with the collector common to the substrate and can be used only in a common collector connection. The N type transistors are four region NPNP's. This actually is a small departure from conventional practice, and the only additional factor to consider is the inclusion of an additional branch in the transistor equivalent circuit for base overdrive current removal by PNP action to the substrate.

Certain types of connections, like the saturated coupling transistor in TTL, operate differently in the NPNP mode. This is not used in 3D, since practically all base overdrive current (a factor of α_p) would be removed by the substrate. On the other hand, operating a grounded emitter NPNP with base overdrive current causes the transistor to "saturate" in a very limited way. The overdrive base current is removed by active PNP action to the substrate. Consequently, the storage time is small ($\tau_s \approx 4$ nsec); the charge represented by the induced base charge of the underlying PNP transistor. However, there are simple modifications to the TTL input coupling transistor (which are shown later) that allow compatibility with the 3D process.

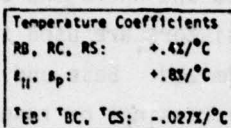
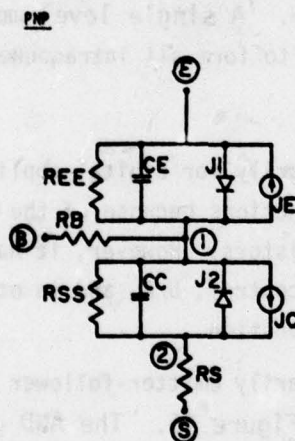
The lateral PNP transistor used in weak interaction technologies is not available in 3D. This is because the strong vertical diffusion gradients restrict transistor action to the immediate vicinity of the device. This works to the advantage of 3D by allowing unrestricted coalescing of NPNP's with PNP's.

This reduced lateral transistor action observed in 3D technology has a benefit with respect to the latch-up phenomena. Latch-up involves PNPN action (not NPNP) for negatively biased substrates and positive biased circuit elements. Because of lateral transistor action in the weak substrate interaction technologies, certain spacing rules and guard ring techniques must be used to avoid this problem. The only precaution for 3D is to ensure a well-grounded substrate (requires a back wafer metallization).

Typical 3D device and structure parameters are shown in Table 16. For circuit simulation, these are used with a modified Ebers-Moll model. Figure 45 is a compilation of NPNP and PNP models. These models are found to be adequate (not more than 10% error) for frequencies up to approximately 30% of the f_α rating of the devices. For high current operation, single "standard" 3D transistors are paralleled rather than using interdigitization of base and emitter strips. This departure from epitaxial practice is necessary because the collector spreading resistance determined by a top

TABLE 16. 3D DEVICE STRUCTURE AND RELATED PARAMETERS

	Units	Value
Substrate (P type)		
Resistivity	ohm-cm	0.8
Concentration	per cm ³	2.5×10^{16}
Collector (N type)		
Surface concentration	per cm ³	9.6×10^{17}
Sheet resistance	ohms/ \square	100
Junction depth	μm	4.8
Average mobility	cm ² /volt-sec	386
Average mobility under base	cm ² /volt-sec	441
Base (P type)		
Surface concentration	per cm ³	1.2×10^{19}
Sheet resistance	ohm/ \square	124
Junction depth	μm	2.0
Average mobility	cm ² /volt-sec	54
Average mobility under emitter	cm ² /volt-sec	39.6
Emitter		
Surface concentration	per cm ³	6.5×10^{20}
Sheet resistance	ohm/ \square	7
Junction depth	μm	1.5
Average mobility	cm ² /volt-sec	47
Alpha cut-off frequency		
NPN	MHz	143
PNP	MHz	51
Junction capacitances		
Emitter-base at -3V	pF/mil ²	0.42
Base-collector at -3V	pF/mil ²	0.25
Collector-substrate at -3V	pF/mil ²	0.08
Diffused resistor values		
Emitter	ohms/ \square	7
Base	ohms/ \square	124
Collector	ohms/ \square	100
Pinched collector region	ohms/ \square	472
Pinched base region	ohms/ \square	18K


$$\begin{aligned} a_N &= .967 \\ a_P &= .75 \\ a_{IN} &= .2 \\ a_{IP} &= .01 \end{aligned}$$


$\sigma_{IP} = .01$

Temperature Coefficients

RB, RS: +.4%/°C
R_p : +.8%/°C
T_{EB} : -.027%/°C

$$C = C_0 [1 - V/V_{CNT}]^{-0.4} + \tau] (q/kT)$$
 $V_{BE1} = .78 \text{ V}, V_{BE2} = .75 \text{ V}, V_{BE3} = .73 \text{ V}$

93

N+ collector ring diffusion does not scale with interdigitization. Single standard transistors (NPNP) are operated up to 2 mA each for the saturating inverter type or 4 mA for the nonsaturating emitter-follower or similar type where the collector spreading resistance is not limiting. The PNP transistors are limited to 1.5 mA collector current maximum and are paralleled for higher currents. Also, overdrive base current to saturating NPNP's is limited to 1.5 mA per standard. The reasons for the latter two limitations are the spreading resistance of the substrate and the requirement that the IR drop not exceed the contact potential of emitter-base junctions for proper operation. The silicon substrate material is P type 0.8 ± 0.2 ohm-cm.

The diffused collector resistors are either pinched or unpinched. The unpinched type is normally used for low resistor values and where the circuits are less tolerant to manufacturing variation. The pinched resistors are used in the large majority of cases where the space required is to be minimized. Base and base pinched resistors have been used only in special cases. Undercrossings or tunnels are provided by the N+ diffusion (emitter) directly into the substrate. All transistors, resistors, and undercrossings are guarded by a P+ field diffusion (this amounts to guard ring construction practice) as shown in Figure 45. A single level metallization is used in combination with tunnels and N+ diffusion to form all intraconnections.

6.4 3D CIRCUITS AND PERFORMANCE

The 3D technology has been used primarily for digital applications. It is regarded as less attractive for analog functions because of the limited voltage breakdown and gain-bandwidth of the transistors. However, it has been used in the analog mode to provide reference voltage control, D/A, and in other utilitarian ways to support an otherwise all-digital LSI function.

The digital logic used has been primarily emitter-follower logic (EFL). Typical circuit elements for 3D-EFL are shown in Figure 46. The AND gates are wired-AND made from PNP emitter-followers. The OR gates are wired-OR made from NPN emitter-followers. This type of utilization is reminiscent of diode logic used much earlier. Grounded emitter inverters are used to complete the necessary logic capability and to restore logic "1" and "0" levels.

Restoration of logic level can also be accomplished in the R/S flip-flop shown in the figure. This type of logic is used extensively within the chip and operates with a +3 volt power supply and ground. Typical operational performance for pseudo-noise generators having extensive combinatorial feedback gating using this logic is shown in Figure 47. The noise margin maintained for this low level logic configuration is relatively good, >0.3 volt for worst case conditions, including temperature and end-of-life wearout.

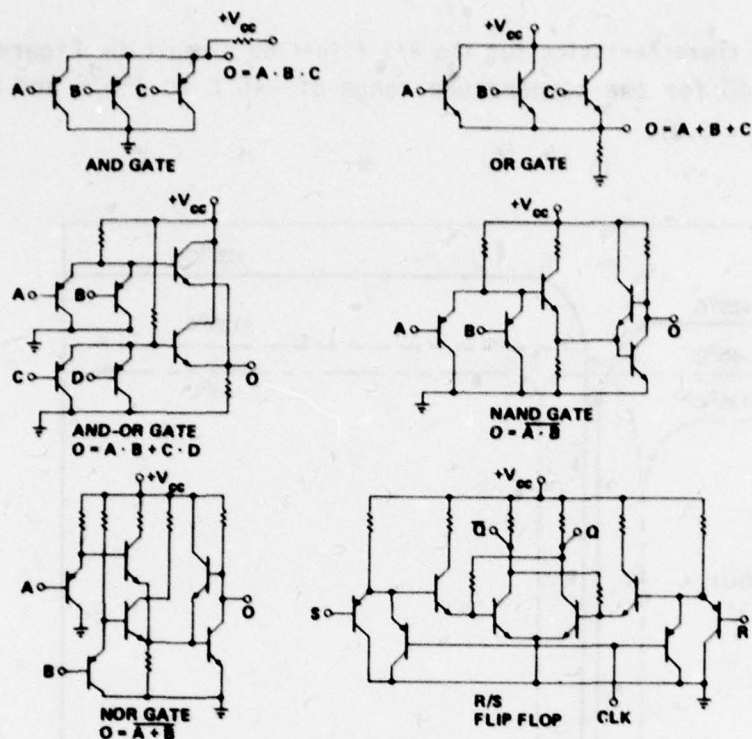


Figure 46. EFL Circuits

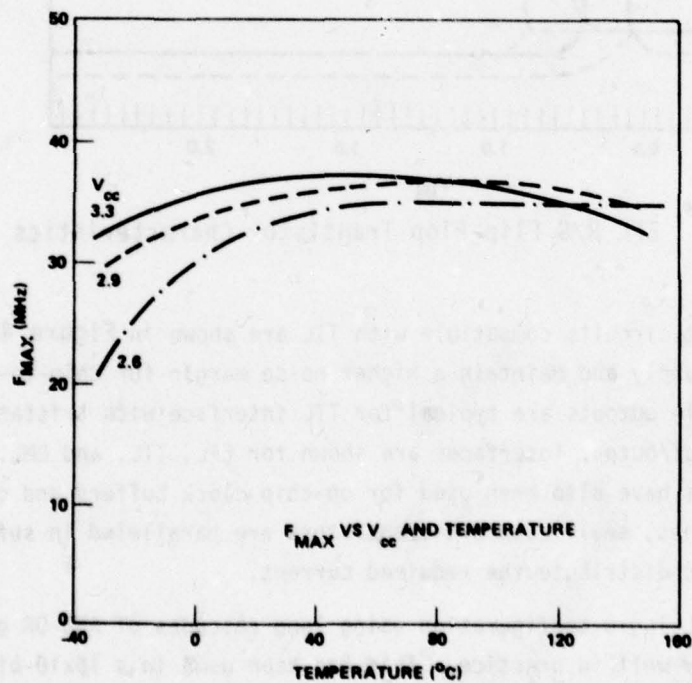


Figure 47. Operational Performance of Typical 3D-EFL LSI vs Temperature and Power Supply Voltage

The transfer characteristics for the R/S flip-flop circuit in Figure 46 are shown in Figure 48 for the temperature range of -40°C to 125°C and under EDL ($\beta_{\text{nnp}} \geq 6.0$, $\beta_{\text{pnp}} \geq 3.0$).

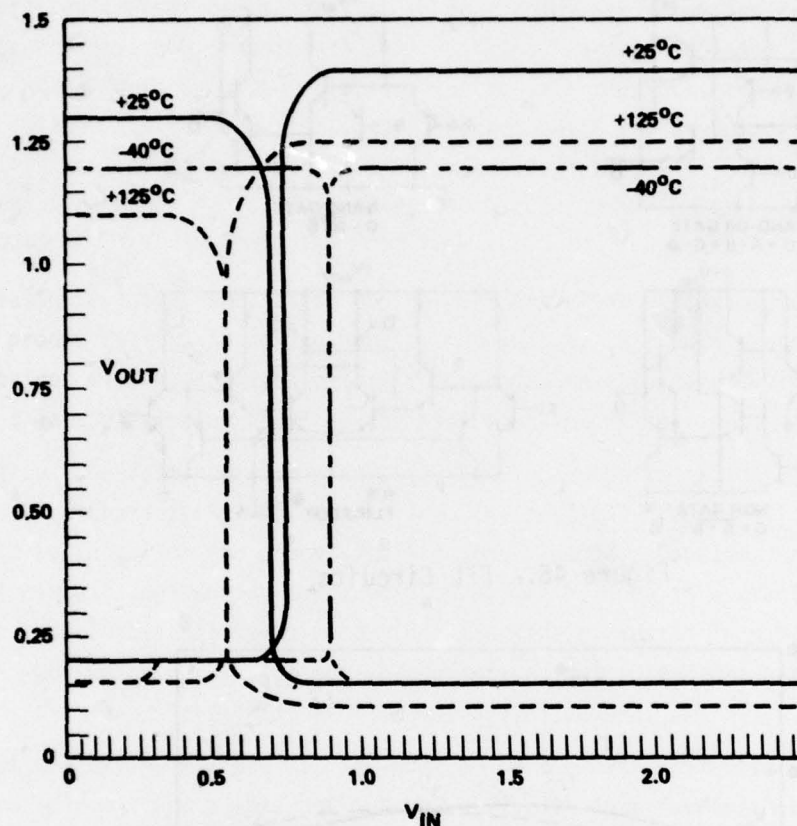


Figure 48. EFL R/S Flip-Flop Transistor Characteristics

Input and output circuits compatible with TTL are shown in Figure 49. These use a 5 volt power supply and maintain a higher noise margin for chip-to-system interface. Totem pole outputs are typical for TTL interface with tristate control also available. Input/output interfaces are shown for EFL, TTL, and CML. Large fanout 50 ohm drivers have also been used for on-chip clock buffers and off-chip loads. For those cases, small standard transistors are paralleled in sufficient numbers to divide and distribute the required current.

A particular EFL logic configuration using long cascades of AND-OR gating has worked out especially well in practice. This has been used in a 16x16-bit parallel multiplier using the successive add algorithm. The logic level is not restored until reaching the product output.

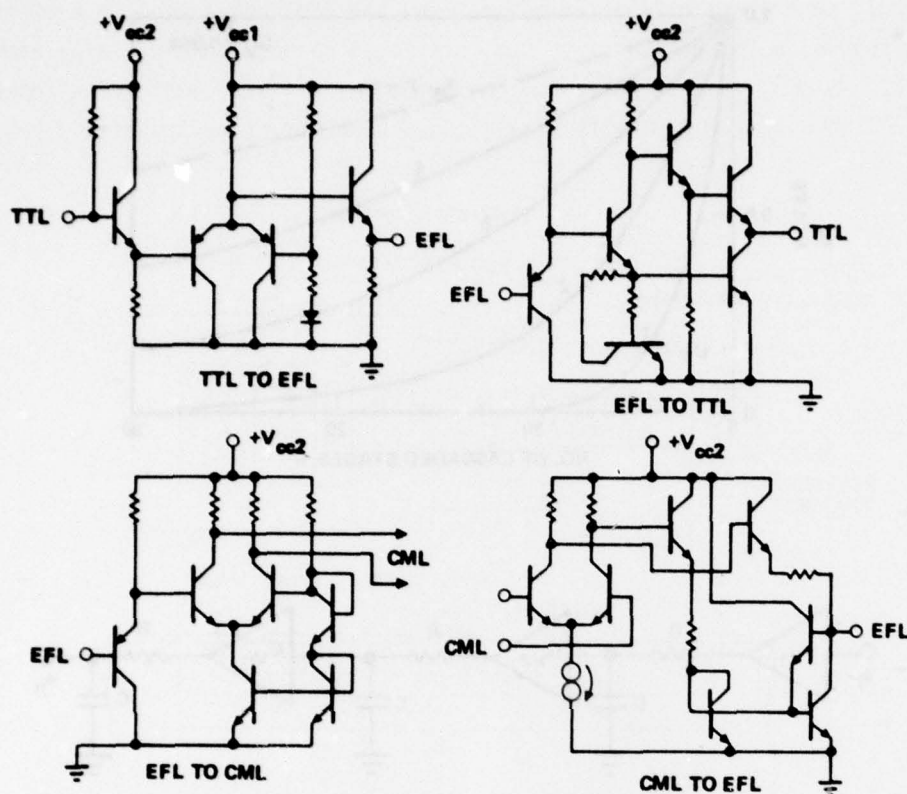


Figure 49. Input/Output Circuits

Throughout the long logic chain, both true and complement signals are generated and propagated. These pairs are finally detected using a differential detector and level restorer at the output. The main advantage of this type of logic chain is found in the reduction of signal propagation time, since the gate delays obey a summation principle which is less than linear summation and approximately RSS summation. As an example, for a low-power full-adder EFL circuit exhibiting a single stage delay time of 14 nsec, a cascade of 32 such stages exhibits less than 100 nsec propagation delay. Figure 50 shows the attenuation and propagation delay as a function of the number of cascaded stages.

Recent extensions of 3D-LSI in the circuit area include current mode logic (CML). This form of logic extends the frequency range to approximately 30% of the alpha cut-off frequency of the devices and exhibits excellent delay-power products. This is a differential form of logic; however, it can also be operated single ended by using a dc reference voltage on one side.

CML can be made compatible with EFL, and there are logic advantages in doing this. CML performs register logic exceedingly well, but has a more limited capability for combinatorial logic. On the other hand, EFL properties are better for gating, and

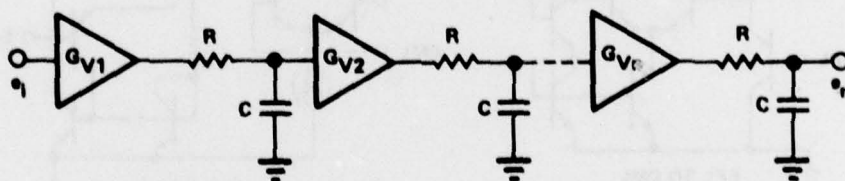
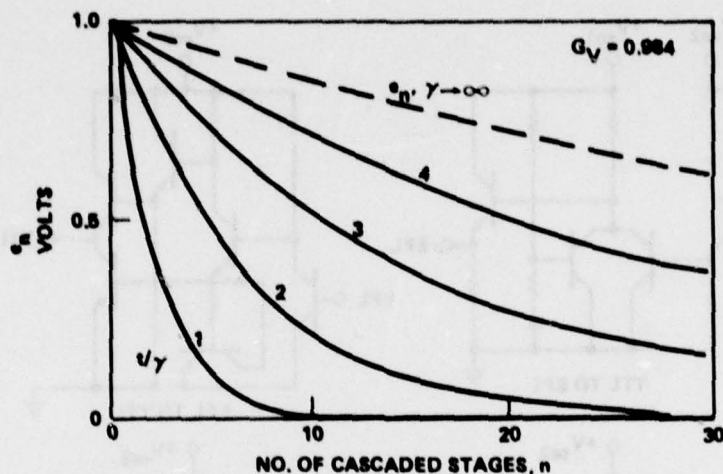


Figure 50. Propagation Delay for EFL and/or Cascade

this is where CML-EFL has an important role. An example of EFL logic to CML D type flip-flop with output restored to EFL levels is shown in Figure 51. This circuit dissipates 32 mW. The setup time is less than 10 nsec, and the propagation delay is 25 nsec for a 80 pF load.

For a long while, it was not realized that a true TTL coupling transistor could be used with 3D. The true TTL coupling transistor operates in a continuously saturated mode in the sense that the base-collector is always forward biased, independent of whether the logic state of the gate is true or false. Under these conditions for 3D, the overdrive base current is diverted to the substrate by the high α_p , $\alpha_p \geq 0.9$ of the 3D substrate transistor action. Figure 52 shows the problem. So it is obvious that 3D cannot be used for TTL. Or is it?

As usual, solutions to long standing problems tend to be simple and of the "why didn't I think of that earlier" category. Figure 53 shows the obvious solution. The addition of resistor R2 solves the problem. Reference to the NPN transistor model shown in Figure 45 reveals that none of the current available at the collector of T1 can be diverted by PNP action to the substrate, and a current like I_2 is therefore fully available for external drive requirements. Resistor values R1 and R2 are

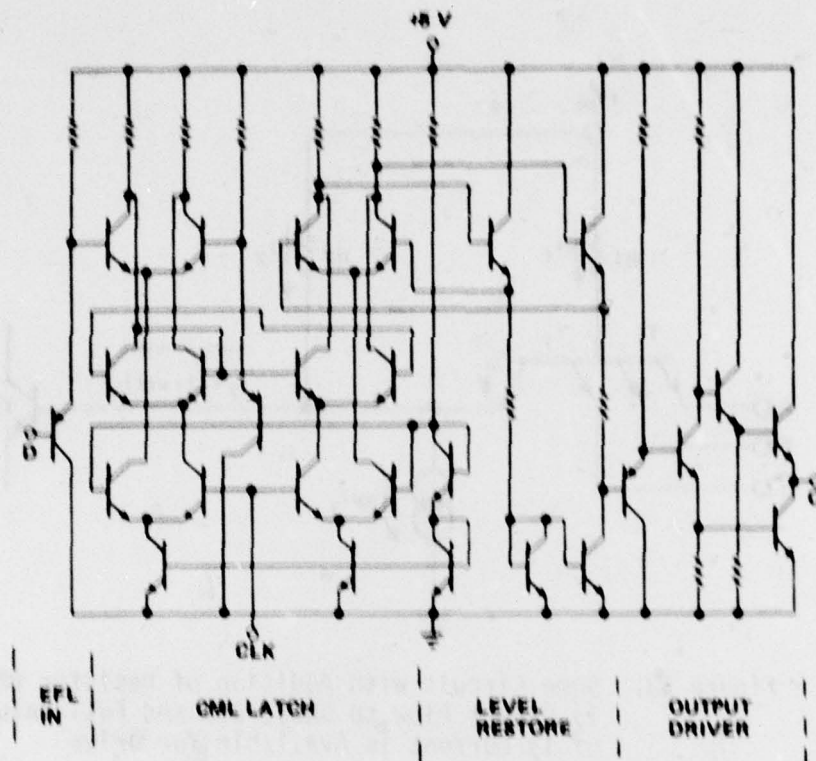


Figure 51. EFL-CML-EFL D Type Flip-Flop

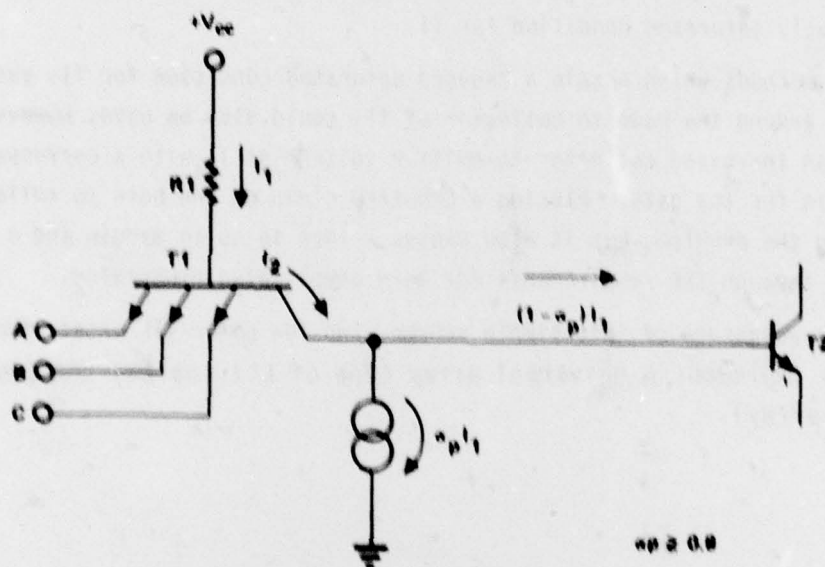


Figure 52. Use of Saturated TTL Coupling Transistor in 3D
Diverts Almost all of Available T1 Base
Current to Substrate, Leaving Only a Small
(1- α_p) Residual for Driving Transistor T2

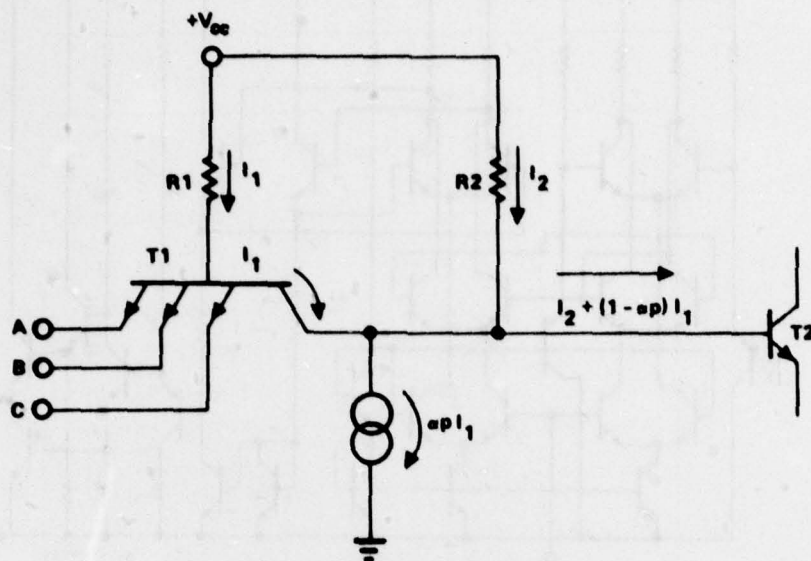


Figure 53. Same Circuit with Addition of Resistor R2.
 I_2 Cannot Flow to Substrate and Full Value
of I_2 Current is Available for Drive

selected to maintain a forced beta of 4, so for this case only 25% of the current is diverted to the substrate. I_1 , of course, performs valuable service by maintaining a continuously saturated condition for T1.

Other methods which obtain a reduced saturated condition for T1, such as shunting a resistor around the base to collector of T1, could also be used; however, these result in an increased collector-to-emitter voltage at T1 with a corresponding loss in noise margin for the gate. Placing a Schottky clamp on the base to collector of T1 would avoid the problem, but it also causes a loss in noise margin and a loss in producibility through the requirements for more complicated processing.

Taking advantage of this simple scheme, two low power TTL gates were designed into 3D to implement a universal array type of LSI, called CGA (for configurable gate array).

Figure 54 shows the schematic diagram for the 3D compatible gate. Typical performance based on test simulations is as follows:

Gate Type 1: $P_{dc(avg)} = 1 \text{ mW}$
 $R_L = 4 \text{ K}$
 $C_L = 30 \text{ pF}$
 $\tau_{pLH} = 30 \text{ nsec}$
 $\tau_{pHL} = 40 \text{ nsec}$

Gate Type 2: $P_{dc(avg)} = 5 \text{ mW}$
 $R_L = 2 \text{ K}$
 $C_L = 100 \text{ pF}$
 $\tau_{pLH} = 30 \text{ nsec}$
 $\tau_{pHL} = 29 \text{ nsec}$

These performance factors are equivalent to those obtained for low power TTL which uses a more complicated process and are consequently much less yield worthy.

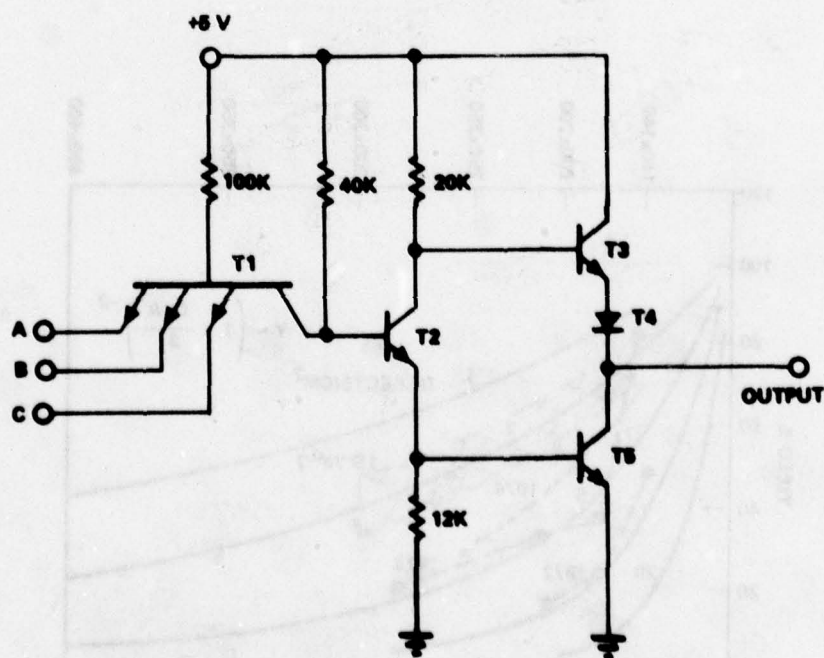


Figure 54. One Milliwatt 3D TTL Gate, $\tau_{pLH} = 30 \text{ nsec}$,
 $\tau_{pHL} = 40 \text{ nsec}$ for $R_L = 4 \text{ K}$, $C_L = 30 \text{ pF}$

6.5 DEFECT FREE YIELD OF 3D-LSI

The singular valid reason for a technology laying claim to being an LSI technology is that it exhibit economic producibility or high yield for complex circuits. A reasonable way to measure the yield and compare this with other competing processes is to construct a graph of chip size (area) versus yield. Using statistical distribution arguments, Dingwall among others has placed a parameter D_0 on such a plot which is descriptive of the number of defects per unit area (cm^2). A series of curves drawn for 3D in Figure 55 shows a progressive trend toward less D_0 , i.e., increased producibility. As shown, this is approximately:

D_0 Defects/ cm^2	Year
10	1972
3	1974
1.5	1976

The yield is plotted for chips passing a functional test at wafer probe, since this is most descriptive of the results of the wafer fabrication process. Subsequent dicing, packaging, visual inspection, and final testing lose approximately 20% beyond the wafer probe test. This is largely independent of wafer processing.

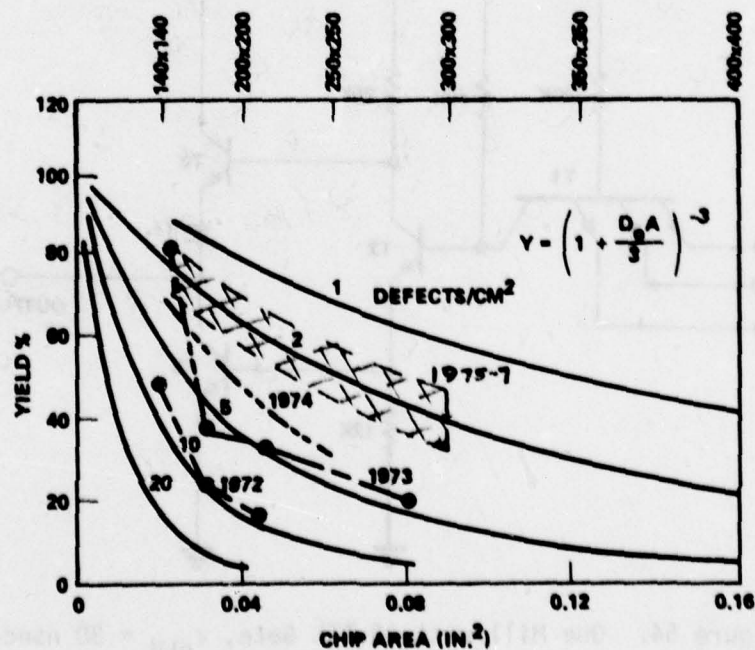


Figure 55. 3D-LSI Yield

Ion implant technology was introduced in 1973 and projection printing in 1975. These account for the decreased defect densities noted.

The 3D technology has reached a degree of maturity in the last 5 years which it failed to do in the previous 14 years. A general resurrection and growth of it is predicted for the future in LSI applications.

The 3D is shown to lend itself readily to different types of circuit technology and interfaces well with existing types. The EFL nonthreshold cascaded gate array, has such superlative performance factors as well as the CML logic and growth of these appear assured for the future.

A general standardization of LSI functions is becoming an increasingly more important subject. Certain subclasses of major system functions, like FFT processing, will be found in single or relatively few chips. These can have the same degree of cost effectiveness that was earlier observed for IC's over discrettes.

SECTION VII

DIGITAL FILTER DEMONSTRATION UNIT, DFDU

The Digital Filter Demonstration Unit, DFDU, is a generalized FFT System that can be used to demonstrate the characteristics of FFT's as well as systems utilizing FFT's. The unit includes an analog preamplifier, a filter, A/D converter, and a VCO for producing modulated FM as well as direct low frequency input signals. It also includes an FM demodulator and audio detector and amplifier. A block diagram display of the DFDU functions is shown in Figure 56. There are basically three overlapped processes implemented in the DFDU: the dual input memory collects 8-bit sampled data at a switch selectable rate and block size.

The other input memory is used to input data to the FFT processor in the first level of operation. The FFT processor performs one butterfly operation at a maximum rate of 480 ns per butterfly in a pipelined fashion and stores intermediate results into its own memory which is 1024 x 24. The process and sample rates are all derived from the programmable system clock. A block diagram of the complete system is shown in Figure 57.

The processor can be selected to perform an N point FFT (where: N=16; 32; 64; 128; 256; 512 or 1024) at a sample rate of

$$S = \frac{10^8}{12(t+1) \log_2 N} \text{ (samples/sec.)}$$

where t is panel selectable from 1 to 999. The window period becomes

$$WP = [12(t+1)N \log_2 N] \times 10^{-8} \text{ sec.}$$

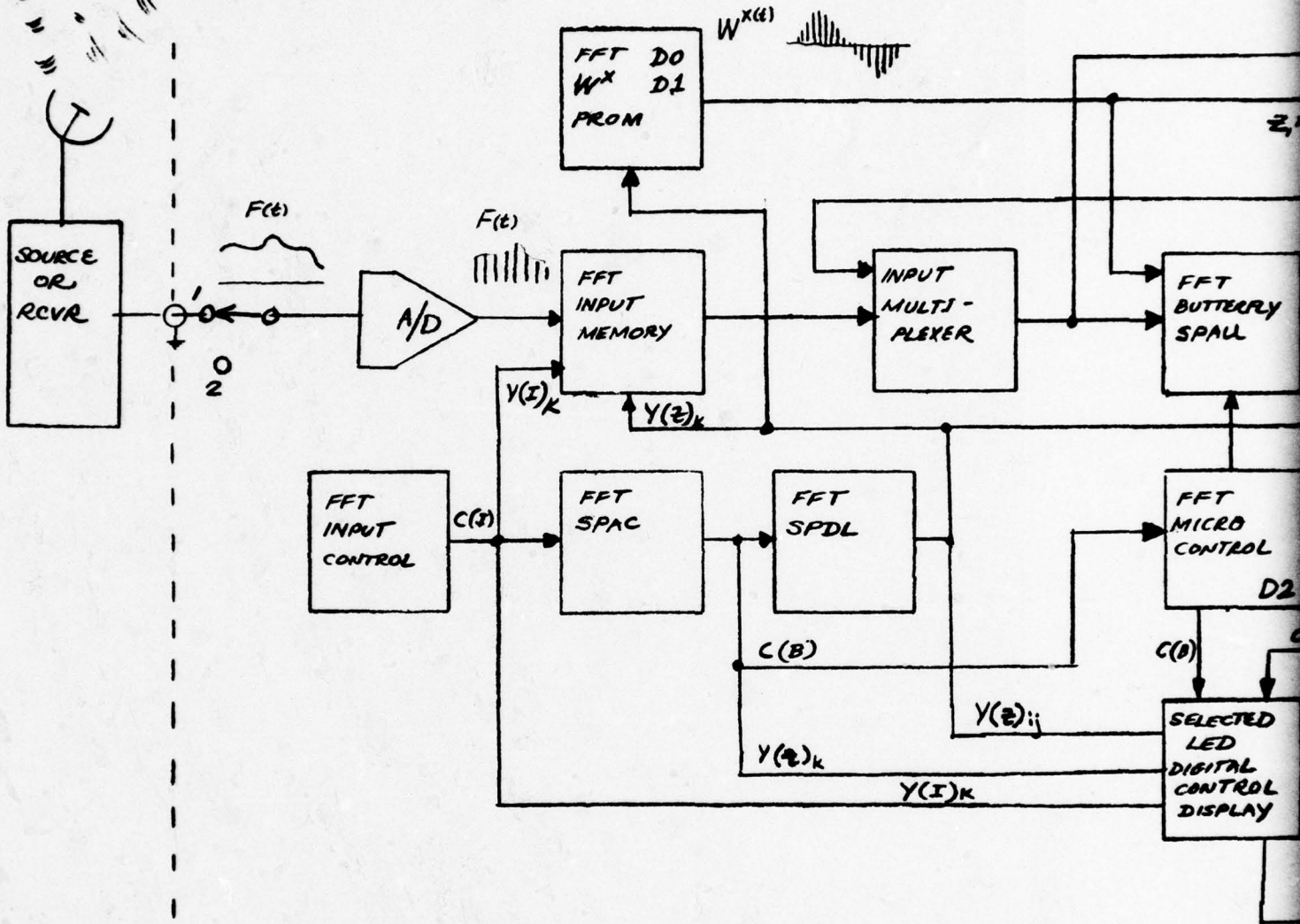
The filter spacing is

$$FS \text{ (filter spacing)} = \frac{1}{(WP)\alpha}$$

$$\alpha = \text{Nyquist Rate, generally } > 2$$

A block diagram of the details of the FFT Kernel Processor is shown in Figure 58.

SK



DISPLAY FOR LSI IMPLEMENTATION
TEST BED FFT

Mode 1 Operation

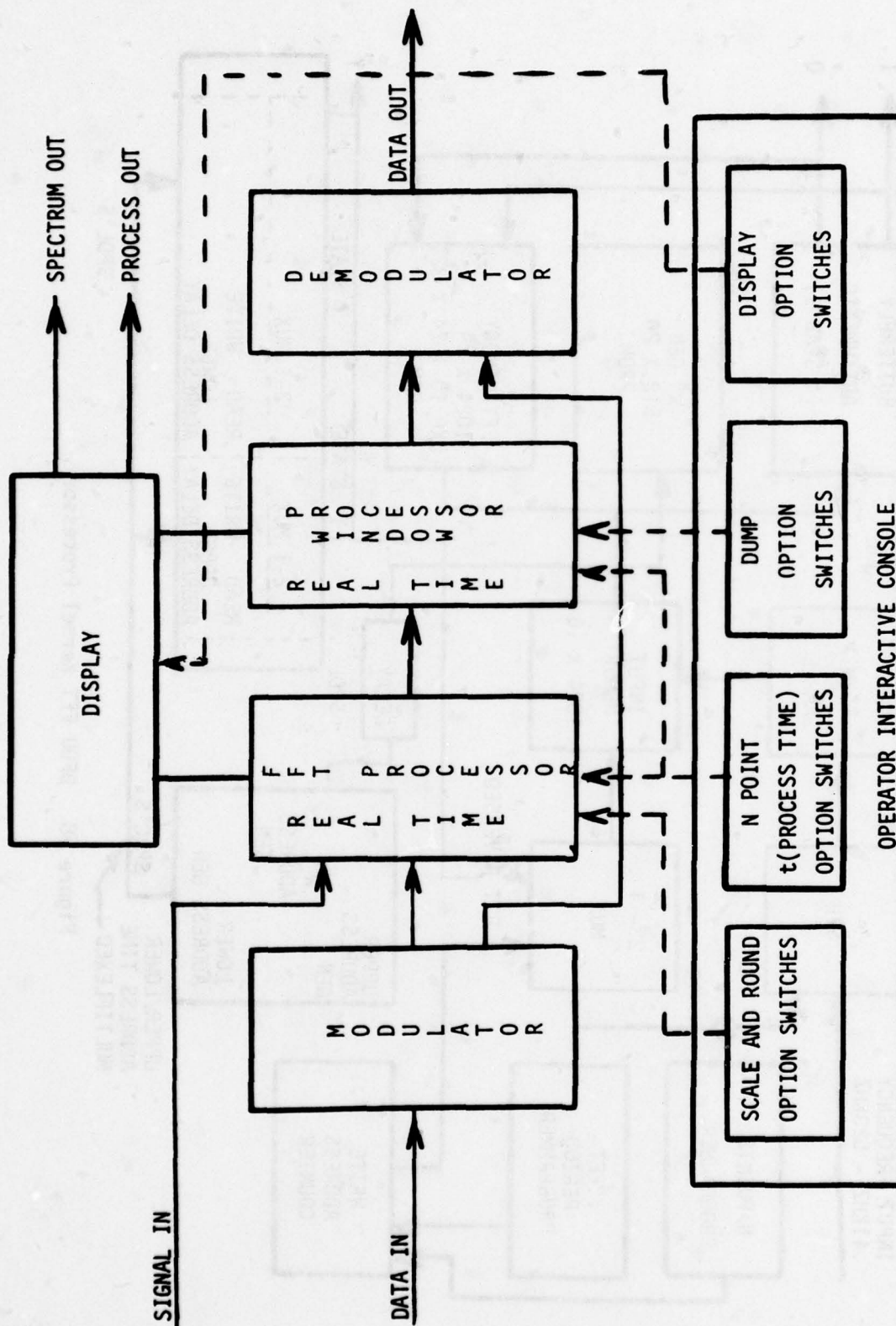
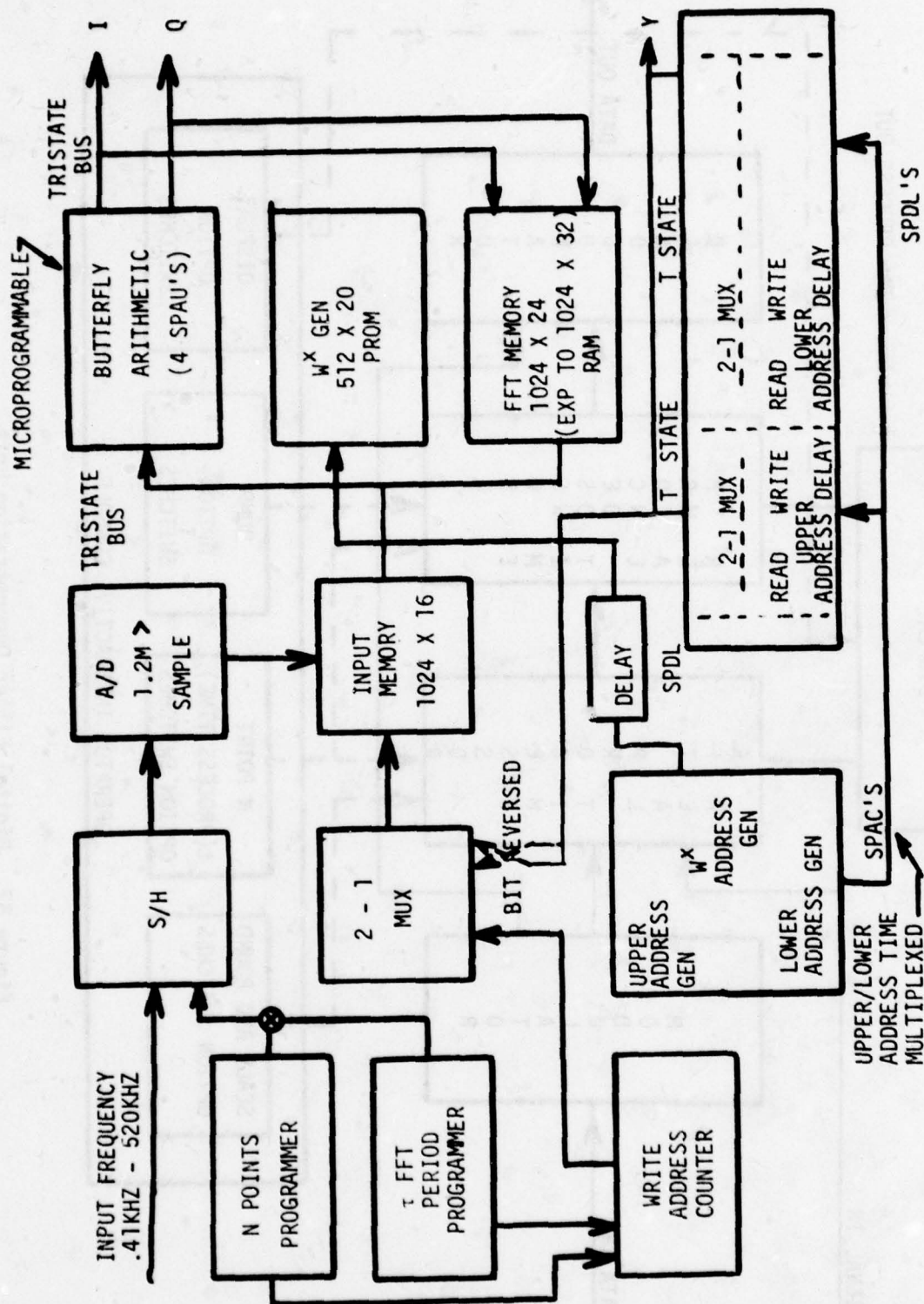


Figure 57. Digital Filter Demonstration Unit



The output of the FFT processor is loaded into the output memory during the last level of the FFT process. The output window processor accesses complex data from its memory and performs the windowing, then it converts the vector to its magnitude and accumulates the outputs over the panel selectable integration interval in the accumulator memory. Figure 59 is a block diagram of the window processors.

The output frequency discriminator processor scans the N frequency components from the accumulator memory and holds the addresses (frequency) of the four largest components.

These values are accessed by queue of the output FM demodulator hardware. The code is used to drive a D/A that drives a VCO for demodulating the input FM signal. These feedback paths may be deleted or bypassed when used in other modes. They serve to self test the DFDU by running it in a closed loop configuration. FFT and window processors and memory busses can be monitored both digitally by samplings at the selected time slot or in continuous operation by monitoring any selected buss through three D/A display channels. There are two digital channels, each channel can select any of several input sources and is useful for maintenance and viewing the process in various levels of its operation, as well as the final output spectrum by the use of an external lab oscilloscope. Figure 60 shows the block diagram for the Maintenance and Display console.

Pictures of the DFDU are shown in Figure 61 through 63. The first shows the stand alone electronics in a cabinet. The second shows the display panel and the third shows the front panel opened to reveal the PC wire wrap construction.

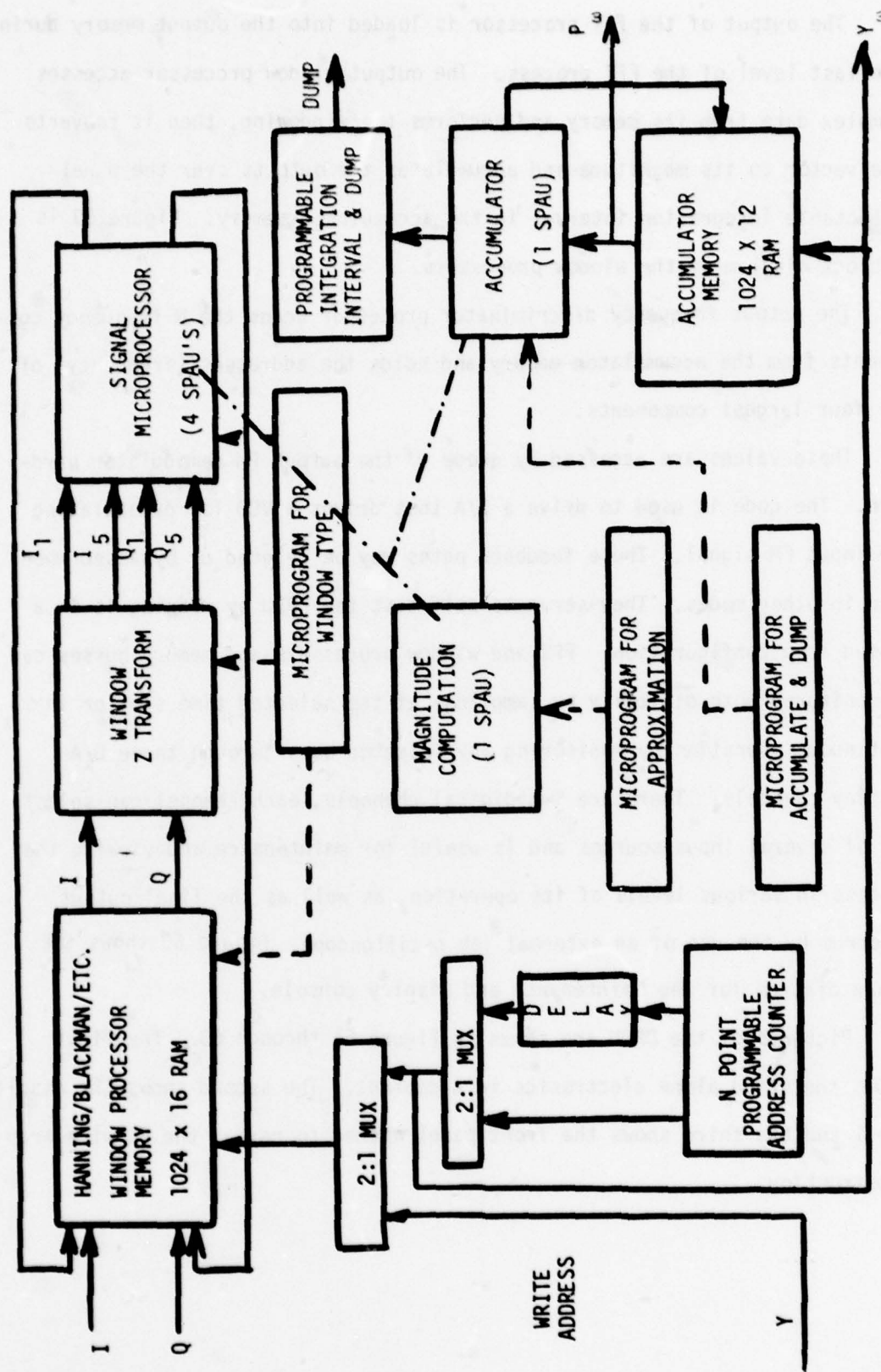


Figure 59. DFDU Window Processor

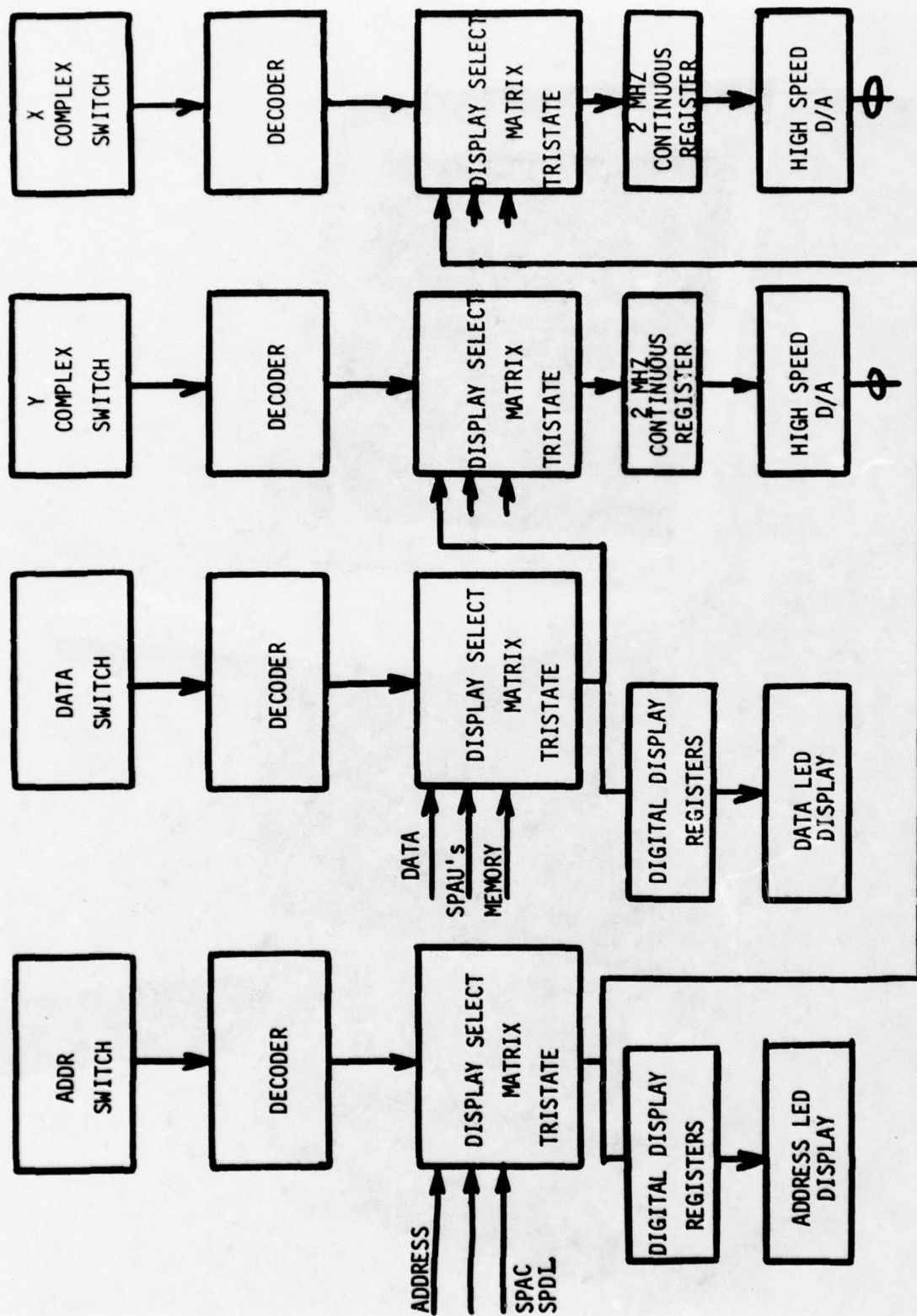


Figure 60. DFU Maintenance and FFT Display Console



Figure 61. Photo of DFDU #128958-76
112

DIGITAL FILTER DEMONSTRATION UNIT AIR FORCE AVIONICS LABORATORY

FFT DISPLAY DATA

LEVEL

FFT DISPLAY LOCATION

ITERATION IN LEVEL

DATA SOURCE

ADDRESS SOURCE

DISPLAY SYNC

RESET

DISPLAY CLOCK

IN

OUT

MAINTENANCE AND EVALUATION DISPLAY

INTEGRATION INTERVAL

SCALE

FFT POINTS

BUTTERFLY TIME

LOG₂N

160 NANoseconds

FFT PERIOD

FREQUENCY

SPECTRAL

POWER

AC

+

+

-

POWER DISPLAY

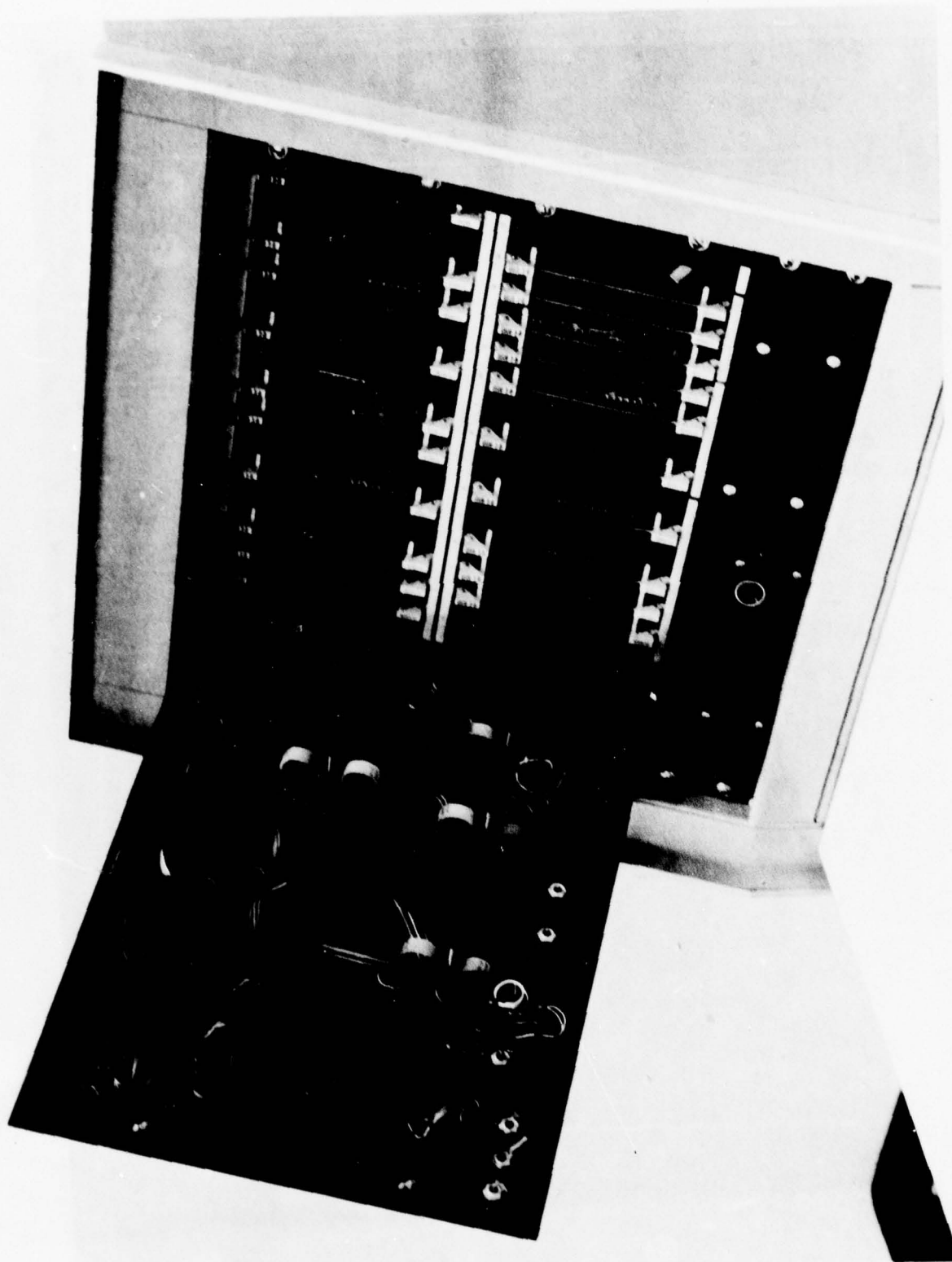
SIGNAL

OPERATION MODE

COMPLEX DISPLAY SELECT

Figure 62. DFDU, Front Panel

#12899-76



#128960-76

Figure 63. DFDI, Internal Construction

SECTION VIII OVERALL CONCLUSIONS

Definitive conclusions were reached in several areas regarding the implementation of LSI for use in digital filter processing applications. These are:

- 1) The LSI replacement of MSI in high arithmetic function density areas such as multiplication-accumulation can show a four to one reduction in power and cost, and one 64-lead LSI package can replace greater than 50 16-lead MSI packages.
- 2) Taken at a major system function level such as an FFT processor, the use of LSI (custom) in combination with MSI (off the shelf) versus an all MSI (off the shelf) results in a recurring cost reduction of 23%. If three custom LSI designs are required for a typical new system of this type the breakeven number of systems is approximately 100 to amortize the development cost. (See section 2.4.)
- 3) For an LSI technology to qualify as a practical cost effective implementation means, the manufacturing defect density must be less than about four defects per cm^2 at a chip level gate density of greater than 100 gates per mm^2 . In 1977 the 3D technology exhibits less than 2 defects/ cm^2 at greater than 200 gates per mm^2 . The 3D technology was the means used for LSI fabrication on this program.
- 4) Given a physical technology as described above in c, the most challenging aspect of the LSI is deriving a suitable partitioning for effective system utilization and thereby specifying the LSI design. A major problem against effective LSI utilization is the limitation in LSI pins available. Sixty to ninety pins is considered the upper limit for reliable inexpensive packaging. The results of this program show that suitable engineering compromise can be reached.

- 5) Practical packaging and handling of power dissipation in LSI over the military temperature range can be realized in 64 lead packages, either flat-pak or DIP and up to 5 watts.
- 6) A general purpose LSI design called the SPAU 2 was shown to be highly effective for all sorts of digital filter generic type problems. This design is based on a multiplier-accumulator type circuit organization. An earlier design called the SPAU(1) was a stepping stone to this final design. Two other hardware designs, the SPDL and SPAC LSI had less general and more specific utilization in FFT applications.

It is apparent from the results of this work that implementation of Avionic systems can greatly benefit from the LSI/VLSI technology. It was shown by means of the delivered hardware on this program that practical technology exists at the required complexity level to meet these needs.

APPENDIX A

SPECIFICATIONS AND APPLICATION NOTES FOR SPAU 1

Note: This was the first Signal Processing Arithmetic Unit, SPAU, designed. This is labeled "SPAU" throughout this Appendix A.

ASSUMPTIONS AND INTRODUCTION

The LSI 3D EFL Signal Processing Arithmetic Unit chip (SPAU) contains control networks, control storage, a 12x12 multiplier, two twelve bit adders-subtractors, a divide by two network, inter-connecting paths and tristate outputs. This specification of the arithmetic unit contains a detailed description of the functions and electrical/delays of the signal processing arithmetic unit.

1.0 FUNCTIONAL

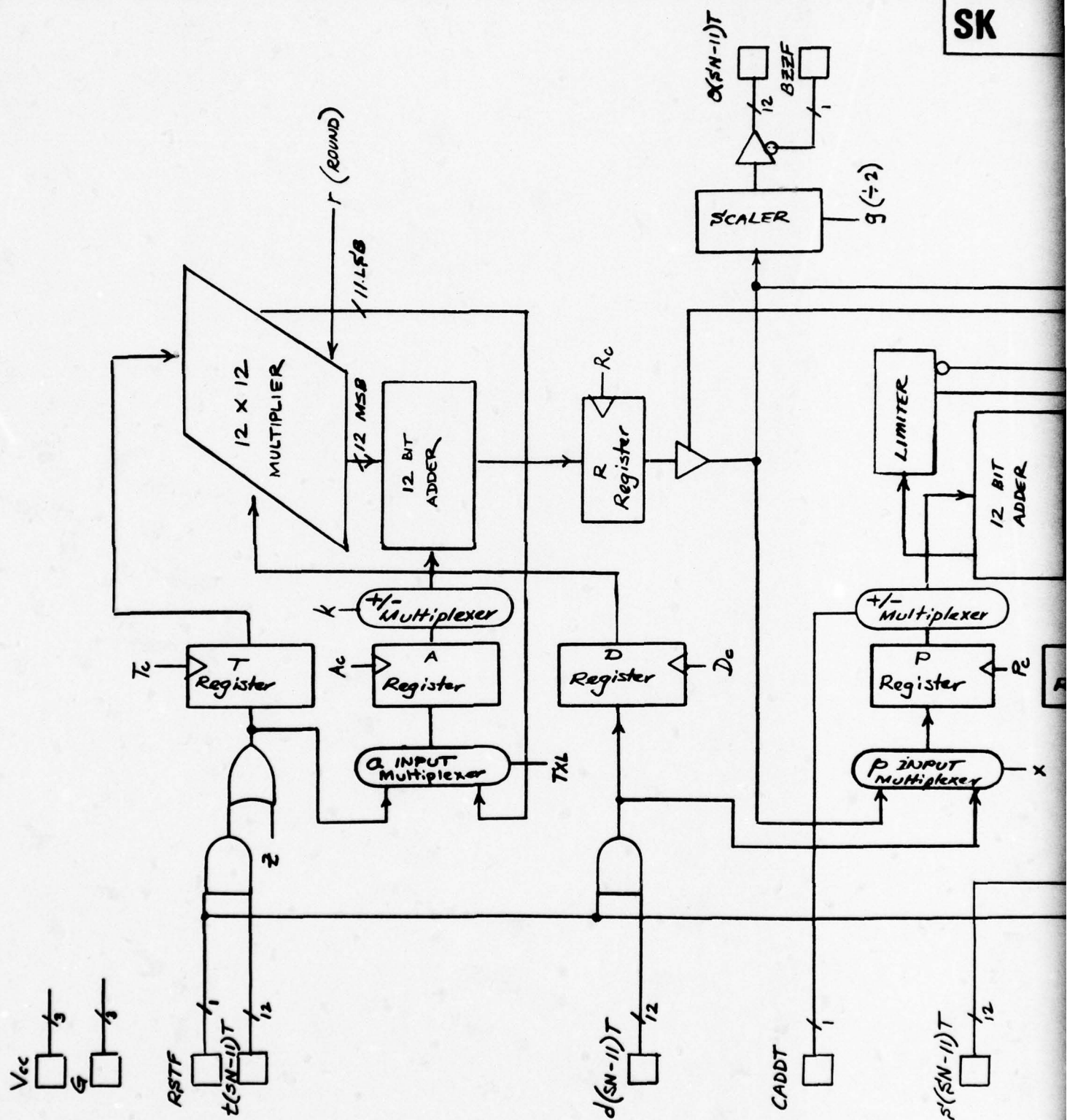
1.1 Operand Holding Registers

There are seven data storage registers contained within the SPAU chip. They receive, load under gated clock, and hold data from pin inputs, internal paths or pin inputs, or arithmetic functions. The registers are placed to provide pipelined processing and may be simultaneously clocked, advancing elements (the function between two clocked registers) along a data pipeline. Table 1 lists the registers and their use. These registers are shown in the functional block diagram Figure 1.

1.2 Configuration Control Register

One register containing five bits holds the configuration control of each SPAU LSI. The configuration register holds the static or low rate data path controls as compared to input pins which drive high rate data path controls. This register is designed in edge-triggered D flip-flops to facilitate overlapped control register, simultaneous control (ROM) address register, and AU configuration register clocking. The function of each low rate control, stored in the configuration register, is given in Table 2. This register is clocked by the C1 control clock. The C1 clock is distributed to all SPAU's in a given configuration. The inputs to the configuration register are time shared with s(SN-11) data, the data lines of lowest use per pipeline period. A pipeline period is the longest time between clocked elements within the pipeline.

SK



SK

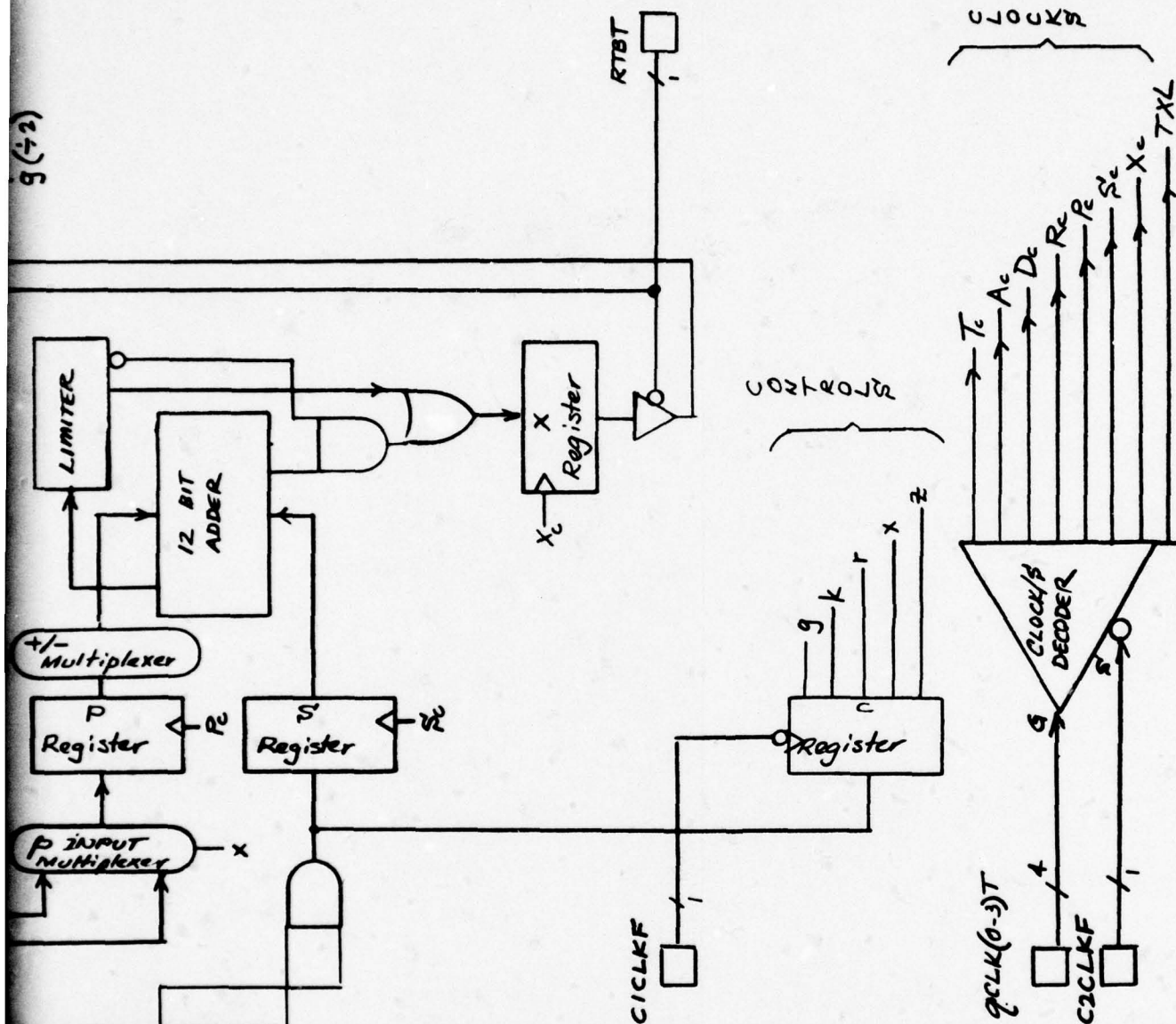
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

Al Whedon

DATE

9/16/75

Figure 1
SPALL Block Diagram

SIZE
B

CODE IDENT NO.
11982

SK

MJO

SCALE 119

SHEET 1 OF

SYSTEMS 3663 REV. 12-71

2

1.3 High Rate Control Lines

There are three control lines which change with sufficient frequency to warrant their independence of timeshared interleaving with data on the s(SN-11) lines. The function of these lines is given in Table 3.

1.4 Data Register Pipeline Clock

The SPAU chip uses a gated continuous clock to strobe-latch-capture data in the pipeline stream. The C2 clock strobes the clock decoder and produces from one to four relatively simultaneous clocks. One pin is allocated for the C2 clock and four pins for the clock code. The sixteen clock codes and the register clocks produced are given in Table 4. The C2 clock is distributed to all SPAU's in a given system configuration.

1.5 Inputs

There are three tristate bus inputs to each SPAU LSI. These are t(SN-11)T, d(SN-11)T, and s(SN-11)T. Each is twelve bits in width representing fractional fixed point two's complement data in the true sense (logic "1"). The distribution of each input is given in Table 5 after the input passes through a synchronous reset override.

1.6 Outputs

There is one TTL compatible tristate twelve bit two's complement fractional output per AU LSI chip. The output source is the internal RX bus passing through a divide by two or normal multiplexer. The data outputs are generated in a logic "1" signal high true sense.

1.7 Multiplier and Adder 1

The multiplier performs two's complement fractional multiplication of the values stored in the multiplier register T(SN-11) and the multiplicand register D(SN-11) forming a twenty-three bit product. The round configuration control bit provides rounding or truncation of the product to twelve of the most significant bits including sign.

TAL - 4
AU CLOCK DECODE CODES

CLOCK CODE	INPUT SELECTS				CLOCKS ENABLED								TXL
	qCLK0T	qCLK1T	qCLK2T	qCLK3T	A	T	D	R _H	P	S	X		
0	0	0	0	0	0	1	0	0	0	0	0	0	
1	0	0	0	1		0	0	0	0	0	0	0	
2	0	0	1	0	0	1	0	1	0	0	0	0	
3	0	0	1	1	0	0	0	1	0	0	0	0	
4	0	1	0	0	0	1	1	0	0	0	0	0	
5	0	1	0	1	0	1	1	0	0	0	1	0	
6	0	1	1	0	0	1	1	1	0	0	0	0	
7	0	1	1	1	0	0	1	0	0	0	0	0	
8	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	0	0	1	0	0	0	0	0	0	0	1	
10	1	0	1	0	1	0	0	1	0	0	0	0	
11	1	0	1	1	0	0	0	0	0	1	0	0	
12	1	1	0	0	0	0	0	0	1	1	1	0	
13	1	1	0	1	0	0	0	0	0	0	1	0	
14	1	1	1	0	0	0	0	1	1	1	1	0	
15	1	1	1	1	0	0	0	0	1	0	0	0	

TABLE 5

INPUTS

INPUT MNEMONIC	RESET OVERRIDE	DESTINATION 1	DESTINATION 2
d(SN-11)T	d(SN-11)F	D(SN-11)R	p(SN-11)T
s(SN-06)T s(07-11)T	s(SN-06)F s(07-11)F	S(SN-06)R S(07-11)R	C(07-11)D
t(SN-11)T	t(SN-11)F	T(SN-11)R	a(SN-11)R

P = P register input multiplexer

C = C	"	"
a = A	"	"
S = S	"	"
T = T	"	"
D = D	"	"

Adder 1 is left justified at (SN-11) in the product range (SN- 22).

Adder 1 is implemented as one level of adder extension beyond the adders forming the partial products. The product and sum are formed simultaneously, their networks being combined. The augend source is $kA(SN-11)$, the one's complement or true value in A plus the carry injection into the adder bit 11 equal a logic "one" or "zero" respectively for subtract or add. The adder 1 add time is equal to the multiply time, approximately 140 nanoseconds from the output of T, D, or A (whichever is loaded last) to the input of R discounting the set-up time for R.

1.8 Adder 2

The second adder in the SPAU is disjoint from the multiplier and adder 1. Its functions operate in full overlap with the multiply and add in the other section and at approximately twice its rate (94 nanoseconds from $XS(SN-11)Q$ or $XP(SN-11)T$).

Adder 2 performs a fast sum and difference for two loaded operands and is used as a self-contained high speed accumulator.

Adder 2 limits for maximum positive and maximum negative overflow. The value (2^0-2^{-11}) is forced into the X register for positive overflow. The value (2^0+2^{-11}) is forced into the X register for negative overflow.

1.9 Reset Override

The periodic reset employed by signal processors in accumulate and dump is implemented as a synchronous reset override at the input $t(SN-11)T$, $s(SN-11)T$, and $d(SN-11)T$. The only cleared register/s is/are those which are clocked during the presence of the reset at the input pin.

TAL 1
OPERAND HOLDING REGISTERS

REGISTER	TYPE	PURPOSE	INPUTS FROM	OUTPUTS TO
A	D-Edge Triggered	Adder 1 Augend Storage	t(SN-11) MPY(13-23)	Add-Subtract Multiplexer Adder-1
D	R-S	Multiplicand Storage Adder 1 Addend Storage when T = 2047/2048	d(SN-11)	Multipplier-Adder-1 Network
P	D-Edge Triggered	Pin Input Adder 2 Addend Storage Product Input Adder 2 Addend Storage Accumulator Return	d(SN-11) or R(SN-11) or X(SN-11)	Adder-2 Network
R	D-Edge Triggered	Product and Adder 1 Sum Storage	Most significant 12 Multiplier Adder-1 bits	RX Inter-register Bus
S	R-S	Adder 2 Augend Storage	s(SN-11)	Add-Subtract Multiplexer Adder-2
T	R-S	Multipplier Storage	t(SN-11)	Multipplier Network
X	D-Edge Triggered	Adder-2 Sum Storage	Adder-2 Sum	RX Inter-register Bus

Table 2
CONFIGURATION CONTROL REGISTER

BIT	TYPE	MNEMONIC	INPUT FROM	STATE	FUNCTION
1	D edge Triggered	g	s10T	1	RX + 2 to output tristate
				0	RX + 1 to output tristate
				f = 0	RX + 1 to output tristate
2	D edge Triggered	k	s08T	0	Carry input bit 11 adder 1 and ones complement A (subtract)
				1	Add A to D+T
				f = 0	
3	D edge Triggered	r	s11T	1	Carry into bit 12 multiplier = 1 or carry propagate (Round)
				0	Carry into bit 12 multiplier = 0 or carry propagate (Truncate)
				f = 0	Truncate
4	D edge Triggered	x	s07T	1	d input to P register
				0	RX bus to P register
				f = 0	RX bus to P register
5	D edge Triggered	z	s09T	1	t(SN-11) = 2047/2048
				0	t(SN-11) = t(SN-11)
				f = 0	t(SN-11) = t(SN-11)

f = Reset override and clock

Table 3
HIGH RATE CONTROL LINES

CONTROL LINE MNEMONIC	STATE	FUNCTION
RTBT	1	Select R (SN-11) to RX(SN-11)B
	0	Select X(SN-11) to RX(SN-11)B
CADOT	0	Select Complement P(SN-11) to Adder 2 Carry in Adder bit 11 = 1
	1	Select P(SN-11) to Adder 2 Carry in Adder bit 11 = 0
bzz F	1	0(SN-11)T tristate outputs selected OFF (FAST OFF)
	0	0(SN-11)T tristate outputs selected ON (SLOW ON)

2.0 ELECTRICAL

2.1 Registers

The SPAU 3D-EFL LSI chip contains eight registers, five single rail D edge triggered flip-flops and three full clock dual rail R/S latches. The specifications for inputs to these EFL implemented registers are given in Tables 6 and 7.

The clocking of these registers is performed by a strobed, decoded clock select. The clocks to the eight registers are enabled from a four bit select code presented to the clock decode input of the AU, Table 4.

2.2 Clock Select Codes

The timing of the clock select codes and clocks is given in Figures 2 and 3 and the tolerances of the clocks are given in Table 8.

2.3 Tristate Outputs

The tristate outputs of the SPAU are specified as follows. This states a capability of a 25 nanosecond risetime for a maximum a.c. load of 50 pF in conjunction with a d.c. load of 6 EFL or two 54S loads.

The use rule is or will be a d.c. maximum of four low power Schottky loads, three bused outputs for 24 picofarads of "off"-output device capacitance (12 per) and 24 picofarads of input device capacitance (6 per), and no more than 10 picofarads for interconnect. (30 pF at 10 inches using laminants 28 mil thick.)

The tristate outputs of the SPAU are specified in Table 9 and Figure 4.

A low input at BZZF enables the tristate device and the OnnBT outputs are inverse of the state of the internal bus RXnnB. This provides a faster disable than enable for the tristate devices and insures compatability with other 54125 devices or AU's on the bus.

2.4 Data Inputs

The SPAU chip has three twelve bit input paths. The "tSNT-t11T" path inputs to an overriding clear gate of one d.c. load. The "dSNT-d11T" path

inputs to an overriding clear gate of one d.c. load. The "sSNT-sllT" path inputs to an overriding S clear gate of one d.c. load. The specifications for these inputs are given in Table 10 and Figure 3.

2.5 Select Control Inputs

The high rate control select inputs drive two type two inverters. The specifications for these inputs are given in Table 11, 13 and Figure 5.

2.6 Configuration Control

The low rate control selects are held in the configuration control D edge triggered flip-flops. This register receives complemented s inputs and is clocked by the control clock. The specification for this register is the same as the D flip-flop specification in Table 6. The propagation delays to the using destinations are given in Table 12 as illustrated in Figure 6.

2.7 High Power Drive External Requirements

One input line is heavily loaded on each SPAU. This line is listed in Table 13 for the proper choice of external drivers.

2.8 Supply Power

The predicted power requirements of the signal processing arithmetic unit (SPAU) LSI are given in Table 13.A.

TABLE 6
D FLIP/FLOP SPECIFICATION

PARAMETER	MNEUMONIC	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5	5.5	V
Clock Frequency	f_C		8	25	MHz
Clock Pulse Width	t_{CW}	15	50		ns
Clear Pulse Width	t_{rw}	$2t_{CW}$	120		ns
Data Hold Time	t_{hold}	5			ns
Q Prop delay-low to high-clock	t_{PLH}		15	25	ns
Q Prop delay-high to low fr clock	t_{PHL}		15	30	ns
Data Set-up D low	$t_{set L}$	15			ns
Data Set-up D high	$t_{set H}$	15			ns

TABLE 7

R/S LATCH INCLUDING SET-UP & TRANSFER GATES

PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
Supply Voltage		4.5	5.0	5.5	V
Clock Pulse Width		30	60		ns
Clear Pulse Width		112	120		ns
Data Hold Time	t_{hold}	60	90		ns
Q Prop Delay-Low to High-Clock	t_{pLH}		50	60	ns
Q Prop Delay-High to Low-Clock	t_{pHL}		22	30	ns
Data Set-up S Low	$t_{\text{set}}^{\text{L}}$	36			ns
Data Set-up S High	$t_{\text{set}}^{\text{H}}$	19			ns

TABLE 8
CLOCK SPECIFICATION

FUNCTION	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
Clock Code Input	Set Up, Input to Strobe	t_{cs}		32	39	ns
	Input High Level	V_{QIH}	2.0	3.4		V
	Input Threshold	V_{QIT}				V
	Input Low Level	V_{QIL}		.3	0.8	V
	Rise Time	t_r		20	30	ns
	Fall Time	t_f		21	30	ns
	Hold Time	t_{hold}	84	120		ns
	Input Capacitance				15	pF
Clock Input (C2CLKF)	Rise Time	t_r		4	8.0	ns
	Fall Time	t_f		4	8.0	ns
	Symmetry Deviation	sym			10	%
	Input High Level	V_{CIH}	2.0	3.4		V
	Input Threshold	V_{CTH}				V
	Input low Level	V_{CIL}		.3	0.8	V
	Skew (Distribution)	t_{skewD}			9	ns
	Strobe & Unload	t_{cu}		30	37	ns
	Skew (Internal)	t_{skewI}			4	ns
	Input Capacitance				15	pF
	Supply Voltage	V_{cc}	4.5	5	5.5	V
	Input Current High	I_{IH}		100	200	μA
	Input Current Low	I_{IL}		-200	-400	μA

TABLE 9
AU TRISTATE OUTPUTS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
OnnBT	Low Level Output	V _{OL}		.25	.8	V
	High Level Output	V _{OH}	2.0	3.4		V
	Supply Voltage	V _{CC}	4.5	5	5.5	V
	Off Line High (2.0V)	I _{OOH}			-50	μA
	Off Line Low (.8V)	I _{OOL}			50	μA
	Off Capacitance	C _O			15	pF
	Drive High	I _{ONH}		.4	1	mA
	Drive Low	I _{ONL}		4	6	mA
	Grounded	I _{OS} *			-30	mA
	Propagation (50 pf, 1K Ω)	T _{PLHI}		25	42	ns
	Delay 25°C	T _{PHLI}		20	35	ns
		T _{PLHE}			22	ns
		T _{PHLE}			22	ns
		T _{PLHD}			25	ns
		T _{PHLD}			25	ns
	Propagation/Temp	T _{PLH}			20%	
	(In Range) 0° - 70°C	T _{PHL}			20%	
	Propagation/Capacitance	T _{PLH}			500	ps/pF
		T _{PHL}			300	ps/pF

*High survival with output at ground.

TABLE 10
DATA INPUT SPECIFICATION

INPUT	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
All	Low Level Input	V_{DIL}		.25	.8	V
All	High Level Input	V_{DIH}	2.0	3.4		V
All	Supply Voltage	V_{CC}	4.5	5	5.5	
t&d	Low Level Input Current	I_{IL}		-100	-150	μA
s	Low Level Input Current	I_{IL}		-100	-150	μA
t&d	High Level Input Current	I_{IH}		125	150	μA
s	High Level Input Current	I_{IH}		125	150	μA
t&d	Input Capacitance	C_I		6	10	pF
s	Input Capacitance	C_I		6	10	pF
t&d to T&D	Reset Propagation Gate	t_{PDLH}		17	30	ns
t&d to J&D	Reset Propagation Gate	t_{PDHL}		19	30	ns
d to p	Reset Propagation Gate	t_{PDLH}		32	45	ns
d to p	Reset Propagation Gate	t_{PDHL}		29	45	ns

TABLE 11
SELECT CONTROL

INPUT	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
A11	Low Level Input Volts	V_{CIL}		.25	.8	V
A11	High Level Input Volts	V_{CIH}	2.0	3.4		V
A11	Supply Voltage Volts	V_{CC}	4.5	5	5.5	V
A11	Low Level Input Current	I_{IL}			-800	μA
A11	High Level Input Current	I_{IH}			200	μA
A11	Input Capacitance	C_I		12	20	pF
A11	Control Propagation	t_{pCLH}		27	35	ns
A11	Control Propagation	t_{pCHL}		17	35	ns

TABLE 12
CONFIGURATION DELAYS FROM CLOCK

FUNCTION	S STATE	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
Scale	1	Propagation Low-High	t_{pLH}		45	72	ns
No-Scale	0	Propagation High-Low	t_{pHL}		45	72	ns
d to P reg	1	Propagation Low-High	t_{pLH}		45	72	ns
RX to P reg	0	Propagation High-Low	t_{pHL}		45	72	ns
T = +1	1	Propagation Low-High	t_{pLH}		45	72	ns
T = t	0	Propagation High-Low	t_{pHL}		45	72	ns
Round	1	Propagation Low-High	t_{pLH}		45	72	ns
Truncate	0	Propagation High-Low	t_{pHL}		45	72	ns
SUBA	1	Propagation Low-High	t_{pLH}		30	47	ns
ADDA	0	Propagation High-Low	t_{pHL}		40	62	ns
s to reg	1	s to config clock	t_{SETL}^*		33	55	ns
s to reg	0		t_{SETH}		35	55	ns

* Assumes 50% derating for worst case timing.

And/Or 15/15

#2 Inverter W/3 loads 25/10

#1 Inverter W/1 load 10/25

Level Resistor Divider 5/5

TPLH/TPHL

TABLE 13

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
RST F	High Level Input Voltage	V_{IH}	2.0	3.6		V
	Low Level Input Voltage	V_{IL}		.3	.8	V
	Input Capacitance	C_I		12	16	pF
	High Level Input Current	I_{IH}		.3	.50	mA
	Low Level Input Current	I_{IL}		-12	-20	mA
	Propagation Time, High to Low Level	t_{PDHL}		10	20	ns
	Propagation Time, Low to High Level	t_{PDLH}		15	30	ns
bzz F	High Level Input Voltage	V_{IH}	2.0	3.6		V
	Low Level Input Voltage	V_{IL}		.3	.8	V
	Input Capacitance	C_I		9	12	pF
	High Level Input Current	I_{IH}		.2	.5	ma
	Low Level Input Current	I_{IL}		-3	-5	ma
	Propagation Time, High to Low Level	t_{PDHL}			10	ns
	Propagation Time, Low to High Level	t_{PDLH}			20	ns

$I_{IL}/\text{Input} = 200\mu\text{A}$; $I_{IH} = 50\mu\text{A}$

* 4pF pad + (2pF x 12 inputs) + 24pF metal

TABLE 13.A
PREDICTED POWER REQUIREMENT

PARAMETER	MIN	TYPICAL	MAX	UNIT
Case Temperature	-40	25	+125	C°
Vcc	4.5	5.0	5.5	V
Power Requirement	3.16	5.14	7.9	W
Icc Total	630	1,028	1,500	mA
Icc per pin	210	343	500	mA
Ri Icc			.1	ohm
per pin			.3	ohm
Vgg Chip - Vgg Package	.060	.103	.150	V
Vcc Chip - Vcc Package	.060	.103	.150	V

3.0 Functional Timing

The maximum propagation times, currents, and capacitances are derated 20% for over temperature performance, $-40^{\circ}\text{C} \rightarrow 125^{\circ}\text{C}$ for any differences in the production of wafers. The typical values are those times expected in performance at 25°C ambient.

3.1 Operation Timing

The Arithmetic Unit (SPAU) executes a function by advancing data elements, generally from a sequential array, through the AU. The input of array-element data, the processing of the previous data element inputs, and the output of a result-element are concurrent operations which are executed in overlap.

3.1.1 Transfer-Element Timing

The loading and dumping of arithmetic unit LSI registers are performed in blocks of time from clock loading source register to clock loading destination register. These blocks of time are called transfer-elements. There are internal and external transfer-elements, those associated with register to register transfer on the same AU and those associated with inputting and outputting into and from the AU, respectively. There are three possible concurrent transfer-elements per AU. Inputs must be held across a delayed clock RS "well", while internal and output transfers are edge triggered and require only a 5 nanosecond "hold time". Table 14 details the worst case and typical propagation delays through the possible transfer-elements. These times are adjusted to reclocking at a common system clock rate, providing margin for excess time in transfer-elements before clock arrival. See Section 3.2 for a discussion of clocks.

3.1.2 Process-Element Timing

There are two process-elements nested between transfer elements and a scaling-element included in the output transfer-element. A process-element spans the time between the leading edge of the clock loading an operand register to the leading edge of the clock latching the arithmetic result register. The process-element is equated to the result register's alpha character mnemonic.

The two process-elements are:

$$R = D * T + kA; k = \pm 1 \quad (1)$$

$$X = S + \ell P; \ell = \pm 1 \quad (2)$$

Both (1) and (2) are overlapping, concurrent processes. Table 15 details the worst case and typical propagation delays through these process-elements. The clocking of transfer-elements also steps data through process-elements. The transfer-elements serve to move data efficiently through cascaded process-elements forming a pipeline. The clock codes serve to step the inputs and outputs of process-elements with one clock with the intent of doing so as close to margins as is practical. In this manner, a given process-element is executed at maximum utility.

3.2 Clocking

The assumed clocking scheme for the system uses a symmetric, complementary two phase clock (one the complement of the other). This permits use of the standard 16.66 MHz oscillator in contrast to two phase asymmetric, noncomplementary clocks generated by a 50 MHz oscillator.

The SPAU uses a clock strobed, decoded clock for each internal register. The clock code is accessed from ROM or PROM one clock cycle before use and is retimed with the clock for use. Retiming should be performed using H or S-TTL propagation speed registers. The 54S194 meets the qualification with margins at both leading and trailing edges of the code. The 54175 & 54174 does not provide sufficient leading edge margin (which is true for EFL also). The 54S174 and 54S175 satisfies the leading and trailing edge cases; however, without trailing edge margin. Tables 16, 17, and 18 and Figures 7, 8, and 9.

A quasi radial clock distribution is required to minimize external clock skew. The limit of 10 nanoseconds is imposed on any stub of the radial fanout. The following limits are established for skew per item per stub.

- | | |
|-------------------------------|---------------|
| (1) maximum 54S140 skew | 4 nanoseconds |
| (2) maximum transmission line | 2 nanoseconds |
| (3) 4 - 30 pf loads | 4 nanoseconds |

The clocking of MSI registers and RAM's in the transfer elements is performed once in 240, 360, 480 nanoseconds by 60 nanosecond slots produced by a ring counter with 60, 120, 180, 240, 300, 360, 420, and 480 nanosecond taps and a recirculate period of 480 nanoseconds.

The selected tap using 54S194's represents a clock offset maximum of 20 nanoseconds using 54128 clock drivers for unloading. The criteria for tap usage is dependent upon worst case propagation delays from a source register through a transfer element to a destination register and the tap or closest timing to a tap used to clock the source register. In the 4AU FFT processor, the most common asymmetric clock from the ring counter has a period of 480 nanoseconds and a pulsewidth of 60. An example implementation for dump X or R to TTL is derived from Tables 14 and 17, and Figure 8. Assume X is clocked by the edge 129 nanoseconds ($92 + 37$) displaced from tap 240's leading edge maximum worst case. Using LS-TTL 170 nanoseconds minimum must be allowed for the transfer element and the tap 60 leading edge, displaced 540 nanoseconds from 0 would clock in data. The transfer time allowed is 300 nanoseconds, the worst case propagation including skew and 20% margin is 299 nanoseconds. The typical propagation time at 25°C ambient is 214 nanoseconds ($111 + 103$).

The C1CLKF clock which strobes the configuration register directly is a gated clock which generally is issued during reset initialization. This gating is application dependent and will not be treated here. Note enter k in Table 15 is the set-up of the configuration register. The C1CLKT clock is delayed a maximum of 22 and a minimum of 10 nanoseconds before being applied to the configuration register. Note that the worst case maximum propagation of configuration set-up using LS-TTL requires 3 clock periods or 180 nanoseconds. Substituting H-TTL reduces the configuration set-up to 2 clock periods or 120 nanoseconds.

TABLE 14

Transfer Elements, Internal

<u>X or R to P (RTBT Static)</u>	<u>t</u> <u>alloc</u>	<u>t</u> <u>max</u>	<u>t</u> <u>typ</u>	<u>L</u>
R Reg CML to EFL		30	20	1
O. C. RX Bus Driver		25	15	
O. C. Bus		30	15	1
P Input Multiplexer		30	19	
P Set-up		15	15	
	<u>240</u>	<u>130</u>	<u>84</u>	
<u>R to P RTBT (1-0)</u>				
External Clock Skew		8	5	
545174 (Control)		17	12	-
External Propagation		8	3	0
RTBT Inverter		22	15	1
O. C. RX Bus Driver		25	15	-
O. C. Bus (to IV)		30	15	1
P Input Multiplexer		30	19	
P Set-up		15	15	
	<u>240</u>	<u>155</u>	<u>99</u>	
<u>X to P RTBT (0-1)</u>				
External Clock Skew		8	5	
54 and 174 (Control)		12	8	
External Propagation		8	3	
RTBT (Double-Inverter)		35	22	
O. C. RX Bus Driver		25	15	
O. C. Bus (to IV)		30	15	
P Input Multiplexer		30	19	
P Set-up		15	15	
	<u>240</u>	<u>163</u>	<u>102</u>	

Transfer Elements, External

<u>Dump X or R to RAM</u>	<u>t</u> <u>alloc</u>	<u>t</u> <u>max</u>	<u>t</u> <u>typ</u>	<u>L</u>
X Register (includes CML to EFL)		30	20	1
O. C. RX Bus Driver		15	5	0
O. C. Bus (to IV)		15	10	0
Scale Multiplexer		15	10	0
Tristate Driver		30	15	1
Output (point to point) Propagate (1.5V)		12	8	1
External Data Propagate		10	5	1
External Clock Skew		10	5	-
Wait for Clock (Margin)		43	102	-
RAM Write Time		<u>60</u>	<u>60</u>	
	240	240	240	

Dump X or R to T, D, A, S

X Register (includes CML to EFL)		30	20	0
O. C. RX Bus Driver		25	15	1
O. C. Bus (to IV)		30	15	1
Scale Multiplexer		15	10	1
Tristate Driver		23	10	0
Output (point to point) Propagate (1.5V)		12	8	0
Reset Override Gate		30	10	0
Set-up D, T, A, S		36	22	0
External Clock Skew		10	5	
Wait for Clock (Margin)		29	125	
Clock Delay (Margin)		40	30	
Hold (60 Minimum)		<u>80</u>	<u>120</u>	
	360	360	360	

Transfer Elements, External

Low Speed

LOAD D, T, S

	<u>t</u> <u>alloc</u>	<u>t</u> <u>max</u>	<u>t</u> <u>typ</u>	<u>L</u>
External Clock Skew		10	5	
54LS174 Data Register		30	20	
54LS157 Data Multiplexer		54	36	
Reset Override Gate		30	10	
Set-up D, T, A, S		36	22	
Wait for Clock (Margin)	180	40	87	
Clock Delay		40	30	
Hold (60 Minimum)	<u>120</u>	<u>69</u>	<u>90</u>	
	300	300	300	

High Speed

LOAD D, T, S

External Clock Skew		10	5	
54LS174 Data Register		17	12	
Reset Override Gate		30	10	
Set-up D, T, A, S		36	22	
Wait for Clock (Margin)	120	27	71	
Clock Delay		40	30	
Hold (60 Minimum)	<u>120</u>	<u>80</u>	<u>90</u>	
	240	240	240	

Dump X or R to TTL

X Register (includes CML to EFL)		30	20	0
O. C. RX Bus Driver		25	15	1
O. C. Bus (to IV)		30	15	1
Scale Multiplexer		10	10	1
Tristate Driver		23	10	0
Output (point to point) Propagate (1.5V)		12	8	0
Set-up 54LS174		30	20	0
External Clock Skew		10	5	-
Wait for Clock (Margin)		<u>70</u>	<u>137</u>	
	240	240	240	

TABLE 15

Process Elements

<u>Load A and Add or</u> <u>Load P and Add</u>	<u>t</u> <u>alloc</u>	<u>t</u> <u>max</u>	<u>t</u> <u>typ</u>	<u>L</u>
P Register including CML to EFL		30	20	1
Add/Subtract Multiplexer		15	10	0
Adder Driver		25	15	1
Add Propagation		112	94	1
CML X Register Set-up		15	15	0
Internal Clock Skew		<u>10</u>	<u>2</u>	-
	240	207	156	
 <u>Load S and Add</u>				
S Register		60	35	1
Adder Driver		15	7	0
Add Propagation		112	94	0
CML X Register Set-up		15	15	1
Internal Clock Skew		<u>10</u>	<u>2</u>	-
	240	212	153	
 <u>Change Add to Subtract</u>				
External Clock Skew		8	5	-
54S174 Control Register (CADDT)		17	12	0
Signal Propagation		3	1	0
AU Control Set-up		35	22	1
2 Multiplexer		30	19	-
Adder Driver		15	7	-
Add Propagation		112	94	-
CML X Register Set-up		<u>15</u>	<u>15</u>	-
	240	235	175	

PROCESS ELEMENTS

Enter k

C2CLK	0	0	
External Clock Skew	8	5	-
54LS295 Configuration (Tristate)	70	47	0
Configuration Set-up (k)	<u>55</u>	<u>35</u>	0
	180	133	87

Change k

C1CLK + Q	0	0	
Configuration to mux	30	20	0
Inverter mux Control	22	15	1
K Multiplexer	15	10	0
Product Driver	25	15	1
Product Propagation	168	140	1
CML R Register Set-up	15	15	
Internal Clock Skew	<u>10</u>	<u>2</u>	
	360	285	217

Load D or T and Multiply

D Register	60	35	1
Product Driver	25	15	1
Product Propagation	168	140	1
CML R Register Set-up	15	15	1
Internal Clock Skew	<u>10</u>	<u>2</u>	-
	360	278	207

TABLE 16
MINIMUM CLOCK STROBE & MAXIMUM CLOCK CODE DELAYS

LEADING EDGE

	CLOCK t_{\min}	CODE t_{\max}	L
Delay to 0° Phase Clock	60		
54S140 Driver Delay	6		
54194 Delay		17	
AU (C2CLKF) Clock Inv.	10		(0-1)
AU Clock Decoder		39	
TOTAL	73	56	
Minus Code Total	- 56		
Difference Margin	17		

TRAILING EDGE

Code Width		120	
Delay to 0° Clock	60		
54S140 Driver Delay	6		
54194 Delay		17	
AU Clock Inverter	7		(1-0)
AU Clock Decoder		39	
Clock Width	60		
TOTAL	133	176	
Minus Clock Total		-133	
Difference Margin		43	

TABLE 17

MAXIMUM CLOCK STROBE & MINIMUM CLOCK CODE DELAYS

LEADING EDGE

	CLOCK t_{\min}	CODE t_{\max}	L
Delay to 0° Phase Clock	60		
54S140 Driver Delay		8	
54194 Delay	10		
AU (C2CLKF) Clock Inv.		20	
AU Clock Decoder	22		(0-1)
TOTAL	92	28	
Minus Code Total	-28		
Difference Margin	64		

TRAILING EDGE

Code Width		120	
Delay to 0° Clock	60		
54S140 Driver Delay		8	
54194 Delay	10		
AU Clock Inverter		20	
AU Clock Decoder	15		(1-0)
Clock Width	60		
TOTAL	145	148	
Minus Clock Total		- 145	
Difference Margin		3	

TABLE 18

TYPICAL CLOCK STROBE-CLOCK CODE DELAYS

LEADING EDGE

	CLOCK t_{\min}	CODE t_{\max}	L
Delay to 0° Phase Clock	60		
54S140 Driver Delay	8		
54194 Delay		15	
AU (C2CLKF) Clock Inv.	15		(0-1)
AU Clock Decoder		30	
TOTAL	83	45	
Minus Code Total	- 45		
Difference Margin	38		

TRAILING EDGE

Code Width		120	
Delay to 0° Clock	60		
54S140 Driver Delay	8		
54194 Delay		15	
AU Clock Inverter	10		(1-0)
AU Clock Decoder		20	
Clock Width	60		
TOTAL	138	155	
Minus Clock Total		- 138	
Difference Margin		17	

4.2.2 Register Clearing

The zero override, RSTF, forces the interpretation of input data to a logical zero at all input registers. The A, T, D, P from d inputs, S, and C registers constitute the resettable set. A clock code in conjunction with a clock generates one clock to these registers and the register/s designated by the clock code are cleared. The codes provided are A, T, D, P, or S alone and T and D or P and S together. The zero override also forces the +2047/2048 override feeding the A and T registers to zero.

The initialization clear is held through one microprogram cycle propagating zeroes through the pipeline at start-up. The programmed clear is used to reset an accumulator after n iterations and is introduced at the inputs during the dump output transfer element. The programmed clear should be applied 60 nanoseconds prior to the clock period and follow that period for 60 nanoseconds to reset a particular register or input register pair. The configuration, C, register may be independently reset with the application of the C1CLK and RSTF. The set-up and hold times given previously also apply to the C register.

4.2.3 Register + 1 Data Override

When the function $T \cdot D + k \cdot A$ is to be used as $(+1 \cdot D + k \cdot A)$ the Z configuration flip-flop overrides the $t(s_n - 11)$ input with +1, 2047/2048; and the T and D register clocks may be generated to load the multiplier with the addend or subtrahend into D simultaneously with +1 into T. The Z configuration flip-flop must be returned to its original state by a high input at S09 and a C1CLK clock.

4.2.4 The -1/2048 Default Input Value

The $t(s_n - 11)$, $d(s_n - 11)$, and $s(s_n - 11)$ data inputs are pulled high (5.0V) by a pullup resistor at the input to the TTL buffers when the inputs are open. This eliminates the external provisioning of pullup resistors provided in high speed system design on unused inputs and permits selective grounding of s inputs for constant configuration when those data inputs are not used. It also provides an opposing data pattern to reset override for dynamic testing.

4.2.5 Product Significance

The product of the two values held in the T and D registers is truncated or rounded to 12 most significant bits including sign, depending on the state of the round, r, configuration flip-flop. The round carry is inserted into the 13th bit (2^{-12}). The 11 least significant bits of the product may be accessed by programming the TXL clock code after loading the multiplier and multiplicand.

4.0 Application

The SPAU is designed to provide a high utility in through-put when applied as a continuous function to a data stream. It is designed to be electrically compatible with any one of the five TTL families, L-TTL, LS-TTL, TTL, H-TTL, and S-TTL, directly interfaced. The SPAU may tie onto a tristate bus or be configured into a direct point-to-point logic network. The internal functions and some interconnect controls are configurable through an internal configuration holding register. The remainder are classified as high rate functions and interconnect controls, and are serviced directly from the microprogram control. The clocking of events within the arithmetic unit is controlled by a clock code obtained directly from microprogram control and strobed by a free running easy to use symmetrical low frequency (8.33 MHz maximum) clock.

The functional features include a 12 X 12 bit multiplier, two twelve bit adders with two's complement add/subtract control, product truncation or rounding to the twelve most significant bits, two 12 bit accumulator registers, four 12 bit operand holding registers with synchronous programmed reset, and a 12 bit post operative scaler. An internal bus links the product and adders, provides a fast accumulator, and satisfies a high speed FFT quarter butterfly or low speed half butterfly capability.

4.1 Signal Processing Architecture

The arithmetic unit SPAU is incorporated in a complex arithmetic microprocessor illustrated in Figure 10. A minimum of two complex arithmetic microprocessors is needed to configure a sequential mode FFT butterfly, Figure 11, where each SPAU serves as a "half-butterfly". The most efficient pipelined FFT butterfly is depicted in Figure 12. It is configured from two complex arithmetic microprocessors each containing two arithmetic unit LSI's, each serving as a "quarter-butterfly".

4.2.1 Register Clocking

The arithmetic SPAU contains input and output holding registers as shown in Figure 1. Data is loaded into these registers with the absence of a reset or preset override when one or more clock decoder gates of 7 is enabled permitting the free running clock to pass through to the register/registers. Clocks are enabled according to the Table 4 from clock code inputs QCLKOT or QCLK3T.

4.3 TTL Family Compatibility

The signal processing arithmetic unit (SPAU) is designed to be compatible within the specified limits of the five families of TTL. Mixing of the families in a design requires the adoption of design rules. The SPAU compatibility is not without reservation, however. SPAU inputs, for example, require from 4 to 8X the normal ($40\mu\text{A}$) source current of TTL for V_{IH} and a reduced sink current for V_{IL} . A $50\text{K}\Omega$ base resistor at V_{IL} typically provides $20\mu\text{A}$ current for the input TTL emitter follower buffer and $\sim 80\mu\text{A}$ source current into the TTL output sink at the data inputs. Control inputs require a larger source current. The SPAU input fan-in is limited by the sourcing capability of TTL.

L and LSTTL have low noise margins and consequently should not be mixed into a system utilizing a lot of noisy and high noise margin S- or H-TTL. It is expected that the low noise generated by L or LS-TTL is more compatible with the internal CML (Current Mode Logic) within the SPAU. An LSI partition of an existing system should translate as many MSI, S and H-TTL to L and LS-TTL (except in the clock code area). The L and LS-TTL families have 200 and 300 millivolt noise immunities for V_{IL} at $+125^\circ\text{C}$ respectively. The SPAU output source and sink capability is in keeping with the L and LS-TTL fan-in requirements. The V_{OL} maximum of .3V is under L and LS-TTL load conditions to a fanout of four.

Table 19 is a representative example of cross TTL compatibility at a single gate level. It is only useful in component selection in implementing a preliminary LSI partition.

All a.c. loads are rated at a maximum of 50 picofarads which translates to maximum "daisy chain" of six single stations (clocks and some MSI to three double stations) and ten picofarads of interconnect. The propagation times for these a.c. loads are listed in Table 19 over temperature. These times are intended for use in worst case over temperature designs and apply to single positive NAND gate structure delays from 1.5V input to 1.5V output. As a design practice, establish the propagation delay at 50pf for those devices selected and use this in delay averaging without permitting the a.c. load to exceed 50pf. Budget 7 picofarads per input load (a Dual J-K has a 4 clock load of 28pf), 10 picofarads per foot for #30 wire wrap, 3 picofarad per inch for 28 mil laminants and interconnect logic. The fanouts given in Table 19 assume 3" of interconnect on a multilaminant board. The 50 picofarad load is a maximum a.c. fanout for the arithmetic unit TTL tristate outputs. A maximum of 15 picofarads is assumed for each "off" tristate driver on a tristate bus.

A high speed register should not fanout to a low speed register if both are clocked by the same clock, as a general rule, since the switching time of the high speed register may be many times less than the data hold time of the low speed register. The L and LS-TTL MSI registers are "slow" registers. The design must guarantee that the minimum delay through logic between fast and slow exceeds, in all cases, the hold time plus maximum clock skew of and to the "slow" register, when a high speed register fans out to a low speed register. The SPAU LSI has a mix of high and low speed registers in it; this was done for reasons of area and power economy. In the process of micro-coding the arithmetic unit clock codes, allow sufficient hold time for the arithmetic unit A, D, S, and T registers; and under no circumstances, allow these to be clocked simultaneously with a source register in a transfer-element where they are a destination register.

The clock strobing the clock decoder in the arithmetic unit is continuous which demands a "no-clock" code for holding registers during a clock. The clock codes, implemented, enable the clock gate for any single arithmetic unit register, groups of registers, or no register (all held). The sequence of clock codes, comprising the microprogram, enables clock pulse "wells" to latch input data streams into the A, D, S, and T registers and enables clock edges to capture output result data into the edge triggered P, R, and X registers. The code sequence of the microprogram is derived from the timing of transfer-elements and process-elements, given in section 3.0 of this specification, to accomplish a particular function. One clock code is required per clock period and the minimum clock period is established at 120 nanoseconds for worst case designs.

A twenty percent increase in throughput can be achieved for systems requiring best commercial practices and operating in a controlled 25°C environment using the typical values given in section 3 of this specification. The structure of the arithmetic unit LSI does not preclude its increased capability in a relaxed thermal environment.

TABLE 19

TTL COMPATIBILITY STANDARD

PARAMETER CONDITION	FAMILY	I_{OH} mA	I_{OS} mA	I_{OL} mA	T_{PLH} ns	T_{PHL} ns	$C_L^=$ 50pf 250C	$C_L^=$ 50pf 250C	T_{PLH} ns	T_{PHL} ns	$C_L^=$ 50pf 250C	$C_L^=$ 50pf 250C	$V_{OH}^=$ 3.7V	$V_{OH}^=$ 2.5	V_{IT} max	V_{IT} max	V_{IH} max	I_{IH} max	I_{IL} ma	I_{IL} H/L	LS-TTL	TTL	H-TTL	S-TTL
		$V_{OH}^=$ 2.5V	$V_{OL}^=$ 0.0V	$V_{OL}^=$ 0.3V	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$C_L^=$ 50pf	$V_{OH}^=$ 3.7V	$V_{OH}^=$ 2.5	V_{IT} max	V_{IT} max	V_{IH} max	I_{IH} max	I_{IL} ma	I_{IL} H/L	LS-TTL	TTL	H-TTL	S-TTL
	L-TTL	-1	-3	5	40-50	35-125	35	32	.5	1.25	10.0	-2	1	2	1	1	1	1	1	1	1	1	1	1
	LS-TTL	-4	-13	6	11-125	11-50	9	10	.6	1.0	20.0	-4	4	4	1	1	1	1	1	1	1	1	1	1
	TTL	-5	-20	16	22	15	14	10	1.0	1.0	40.0	-1.6	6	6	6	6	6	6	6	6	6	6	6	6
	H-TTL	-13	-40	20	10-125	10-50	7	6	1.0	1.0	50.0	-2.0	6	6	6	6	6	6	6	6	6	6	6	6
	S-TTL	-20	-40	19	5 flat	6-50	5	5	1.0	1.0	50.0	-2.0	6	6	6	6	6	6	6	6	6	6	6	6
	LSI-TTL-TS	-4	-8	6	42	35					150.0	.05	4	4	4	4	4	4	4	4	4	4	4	4
	TTL-TS	-6	-30	16	13	18	8	12	1.0	1.0	50.0	-1.6	4	4	4	4	4	4	4	4	4	4	4	4

FANOUTS:	$\frac{50\text{pf} - \text{line cap}}{\text{pf}/\text{input}}$ maximum
I_{OH}	Output source current into load
I_{OS}	Output source current into ground short
I_{OL}	Output sink current from load
V_{OH}	Output voltage high
V_{OL}	Output voltage low
T_{PLH}	Propagation 1.5V input to 1.5V output (.3 to 2.5V in) to (2.5 to .3V out)
T_{PHL}	Propagation 1.5V input to 1.5V output (2.5V to .3V in) to (.3V to 2.5V out)
V_{IT}	Maximum Logic 0 Low input threshold
I_{IH}	Input sinking current
I_{IL}	Input (generally) source current

SK

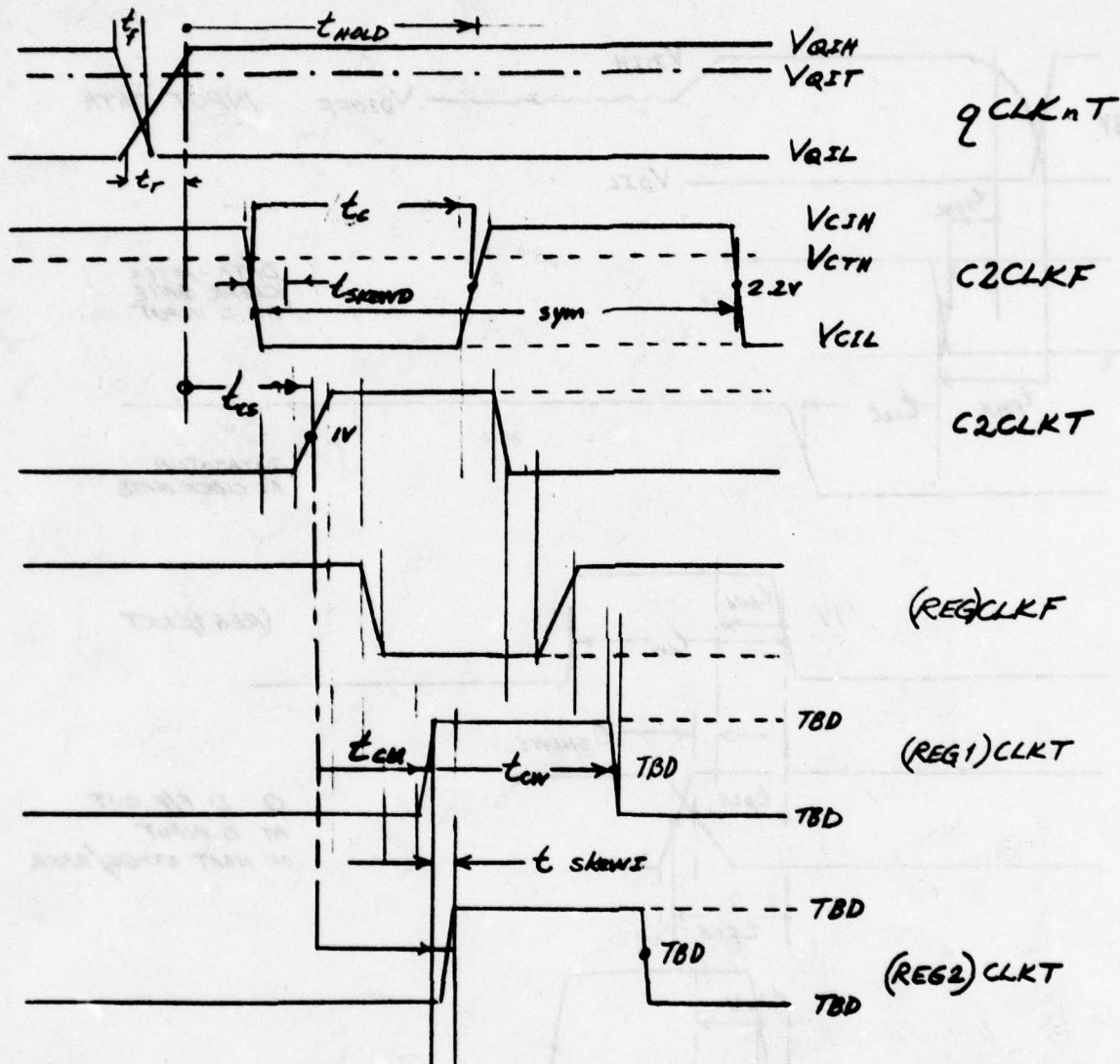
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

ORIGINATOR

DATE

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

Figure 2

Clock to Register D and R/S

SIZE

CODE IDENT NO.

A

11982

SK

MJO

SCALE

157

SHEET 1 OF

SK

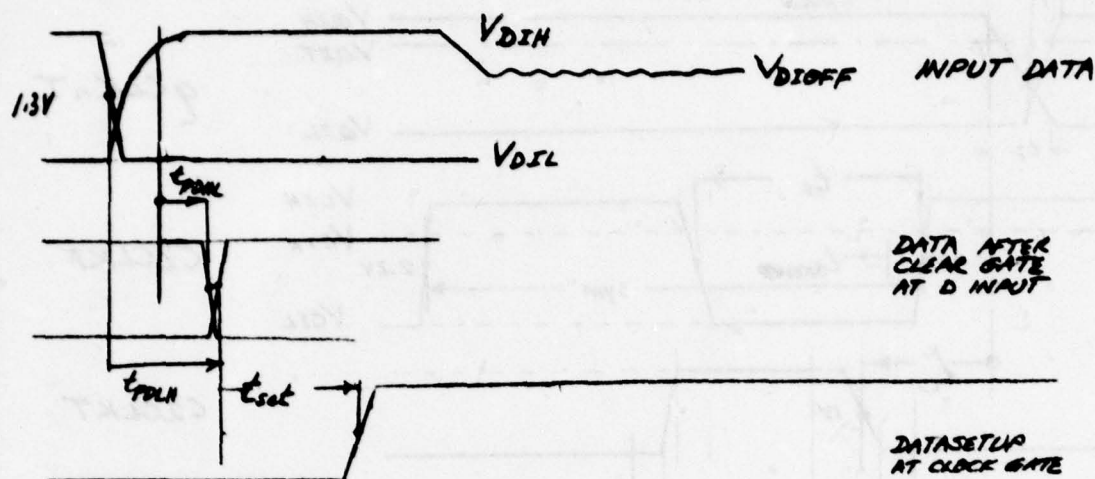
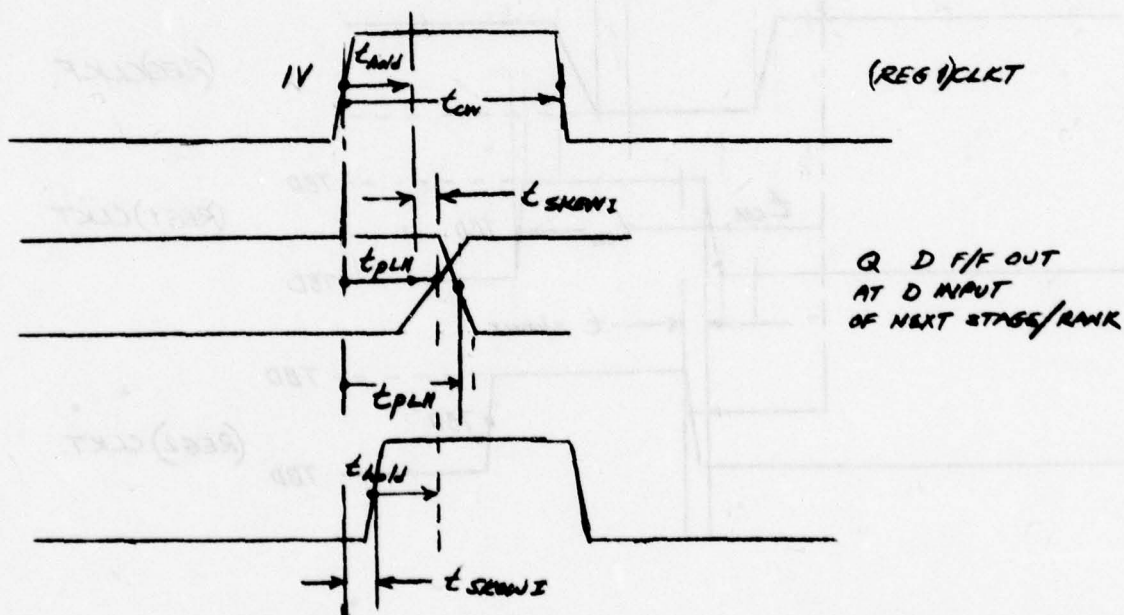
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

DATA AFTER
CLEAR GATE
AT D INPUTDATASETUP
AT CLOCK GATE $(REG) CLK$ Q D f/f OUT
AT D INPUT
OF NEXT STAGE/RANK

ENGINEERING SKETCH

ORIGINATOR

DATE

MJO

TRW

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Figure 3
Data to Register D f/f

SIZE

CODE IDENT NO.

A

11982

SK

SCALE

158

SHEET 1 OF

SYSTEMS 823 REV. 12-71

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

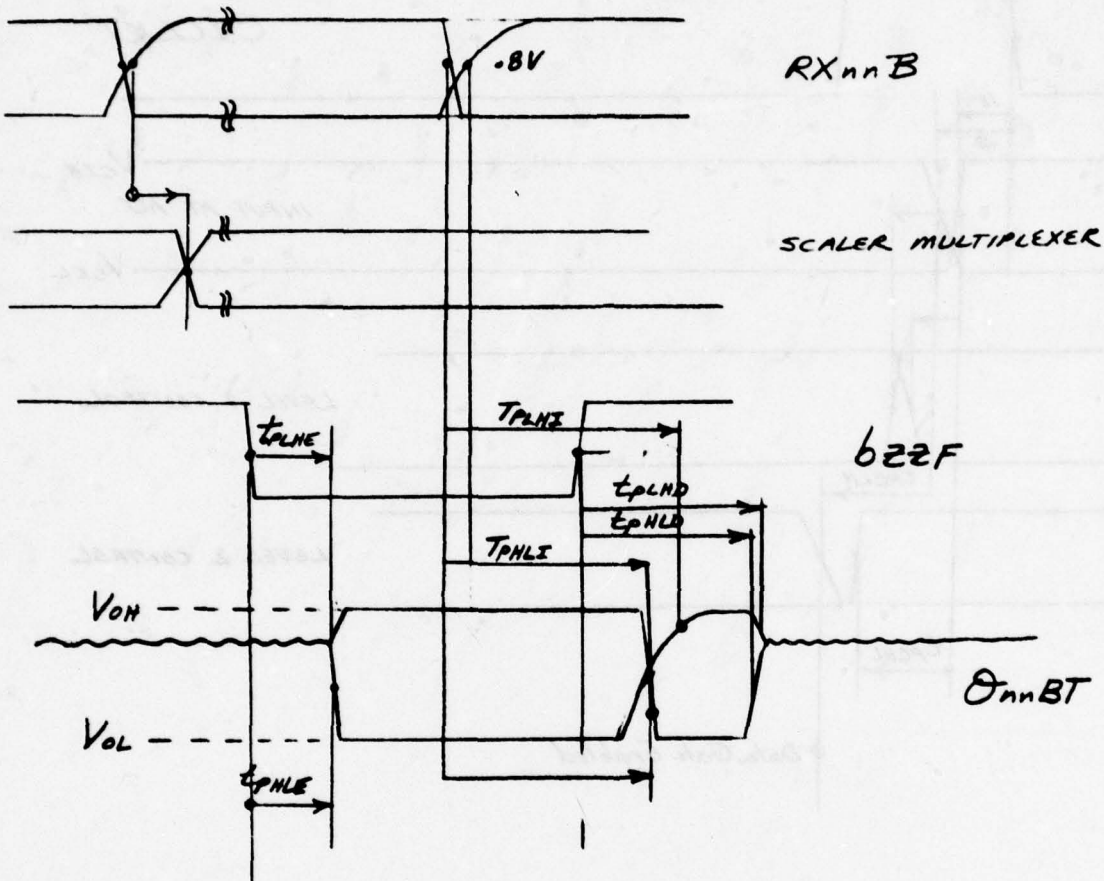
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ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	<i>Figure 4</i> <i>AU Tristate Outputs</i>	
		SIZE	CODE IDENT NO.
		A	11982
		SK	
MJO		SCALE	SHEET 1 OF
		159	

SK

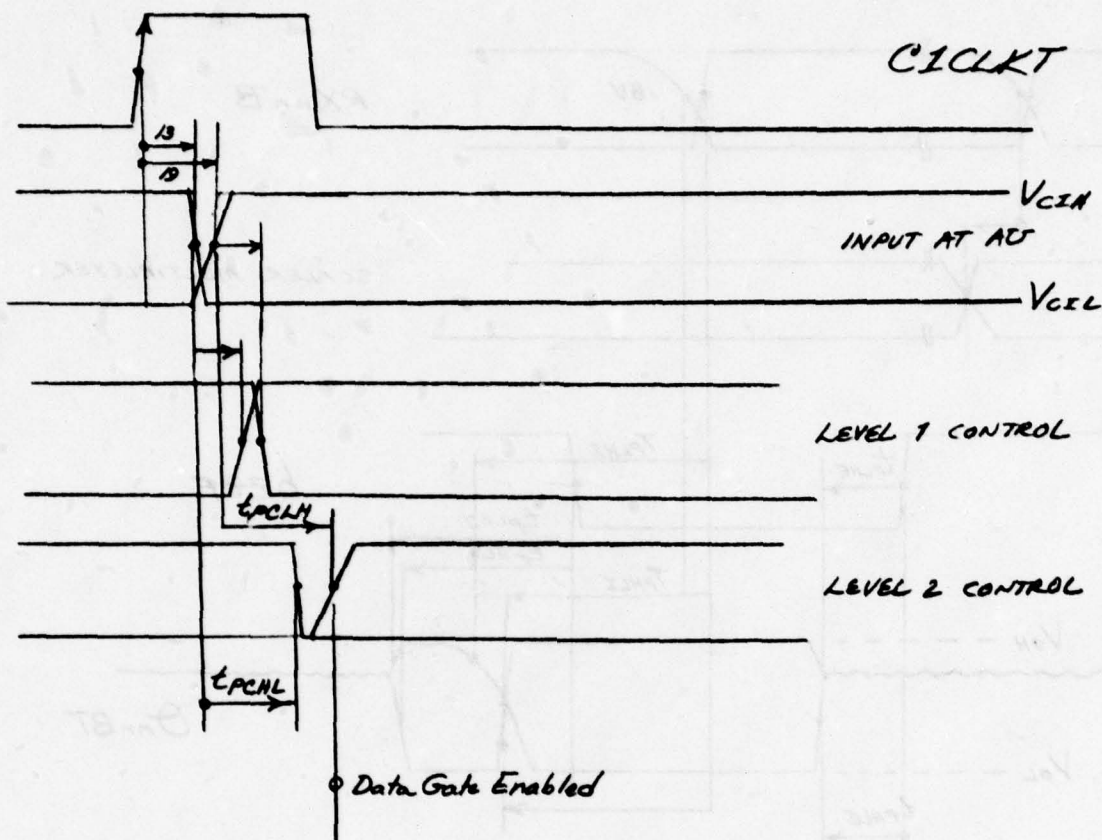
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ENGINEERING SKETCH

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DATE

MJO

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ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

*Figure 5
Select Control*

SIZE

A

CODE IDENT NO.

11982

SK

SCALE

160

SHEET 1 OF

SK

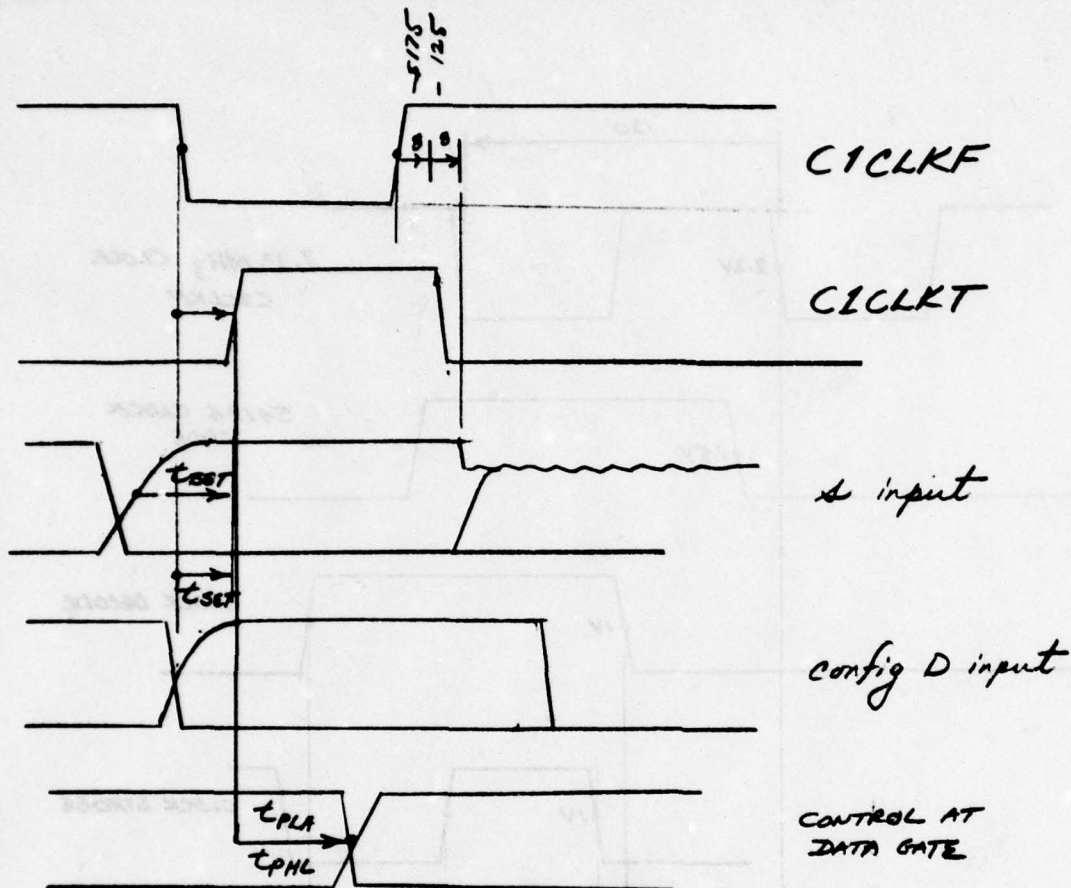
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CONTROL AT
DATA GATE

ENGINEERING SKETCH

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ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

Figure 6
Configuration Control

SIZE

CODE IDENT NO.

A

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SCALE

161

SHEET 1 OF

SK

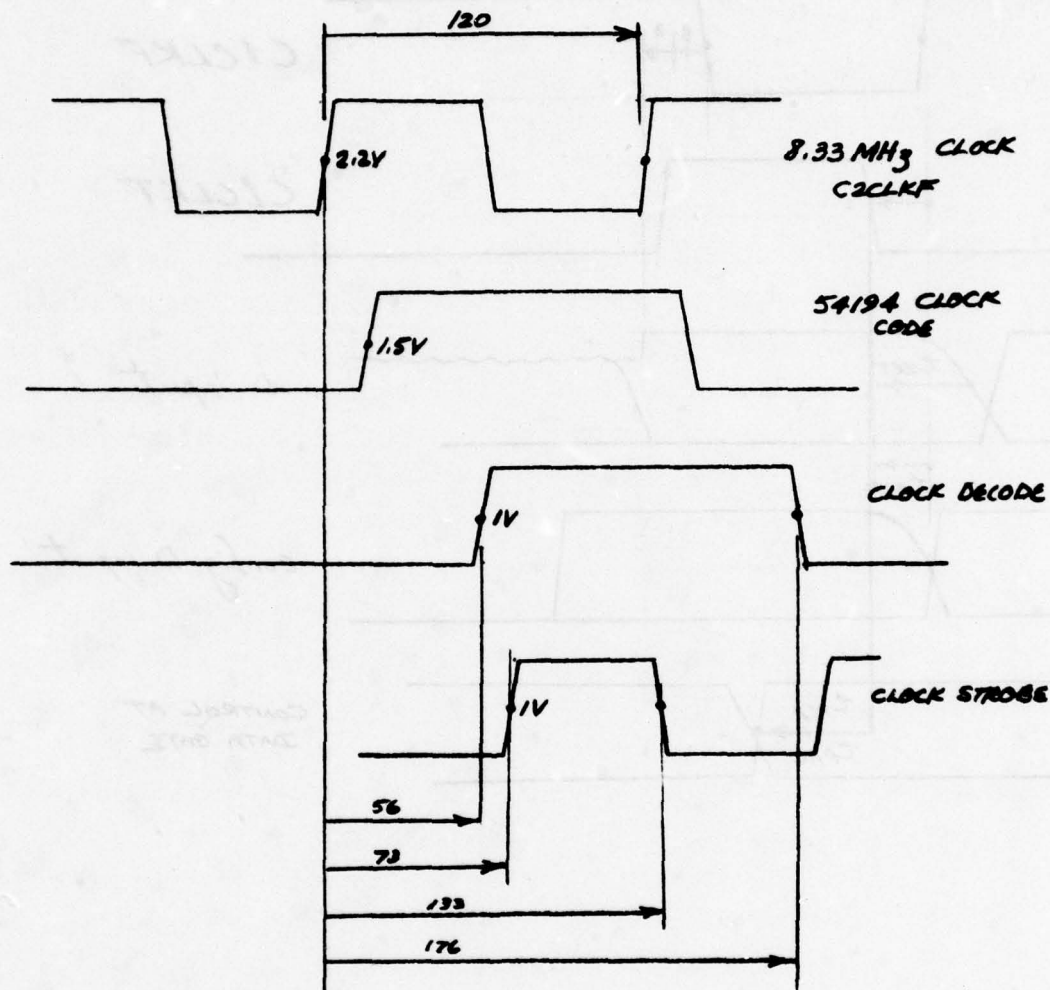
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ORIGINATOR

AL WHEDON

DATE

MJO

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

Figure 7

Worst Case Clock Strobe & Clock Code Timing
Minimum Strobe - Maximum Code Delay

SIZE

A

CODE IDENT NO.

11982

SK

SCALE

162

SHEET 1 OF

SK

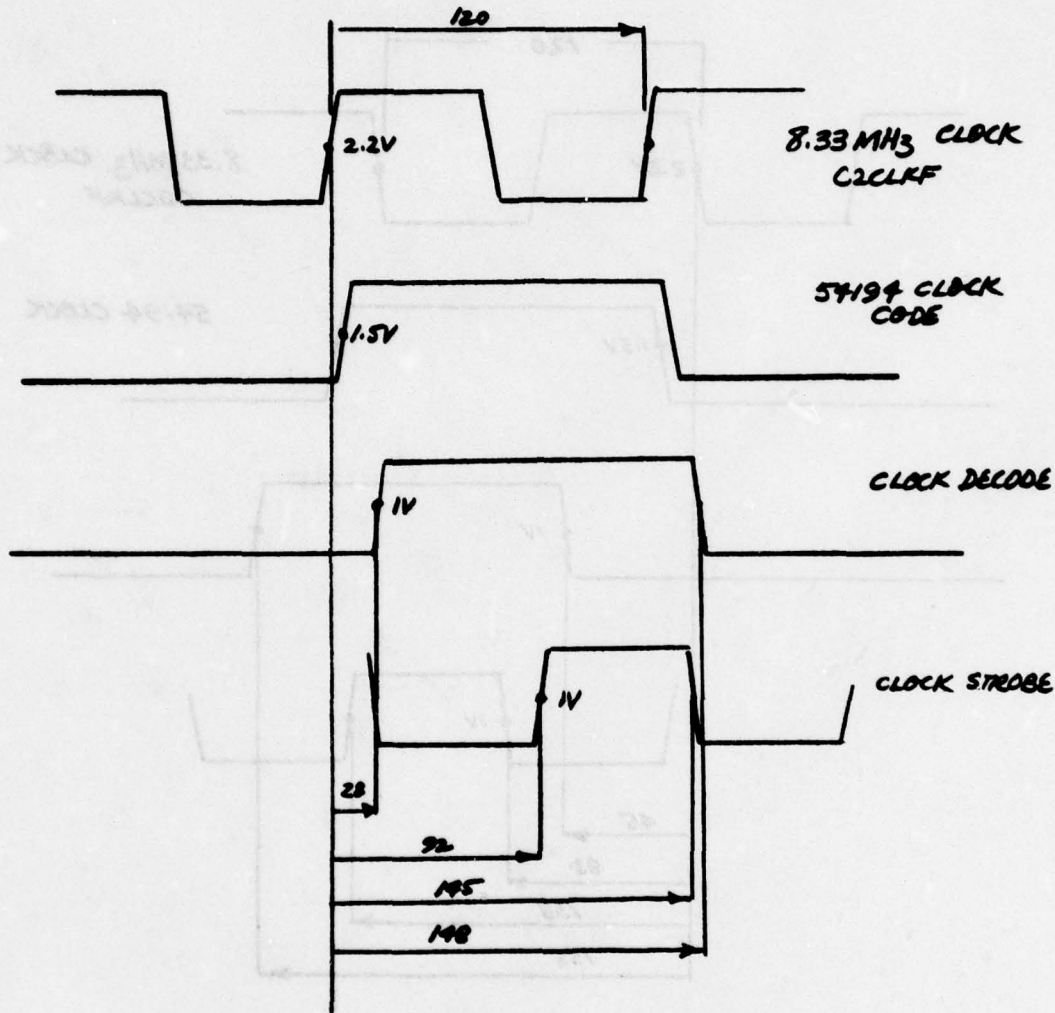
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DESCRIPTION

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ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

AL WHEDON

Figure B
Worst Case Clock Strobe & Clock Code Timing
Maximum Strobe - Minimum Code Delay

SIZE

CODE IDENT NO.

A

11982

SK

MJO

SCALE

163

SHEET 1 OF

SYSTEMS 223 REV. 12-71

SK

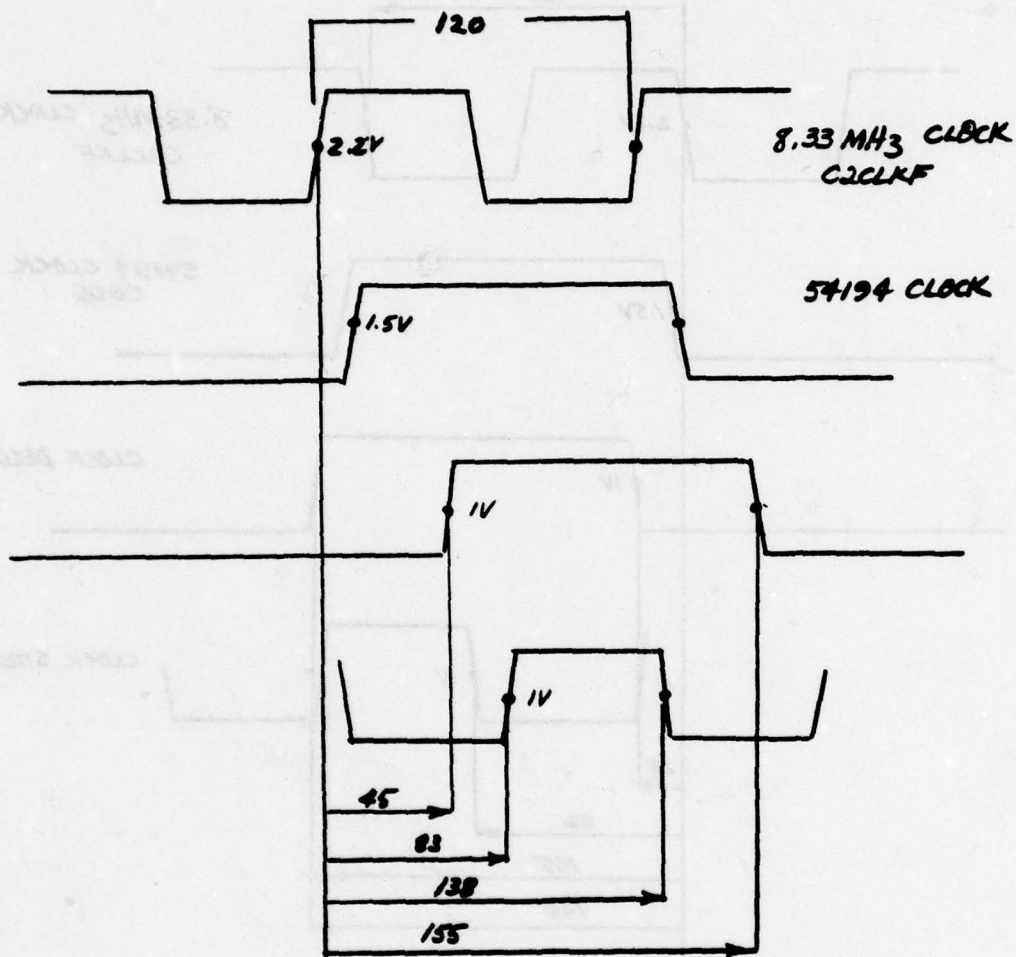
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ENGINEERING SKETCH

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SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

*Figure 9
Typical Case Clock Stroke & Clock Code Timing*

SIZE

CODE IDENT NO.

A

11982

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MJO

SCALE

164

SHEET 1 OF

SK

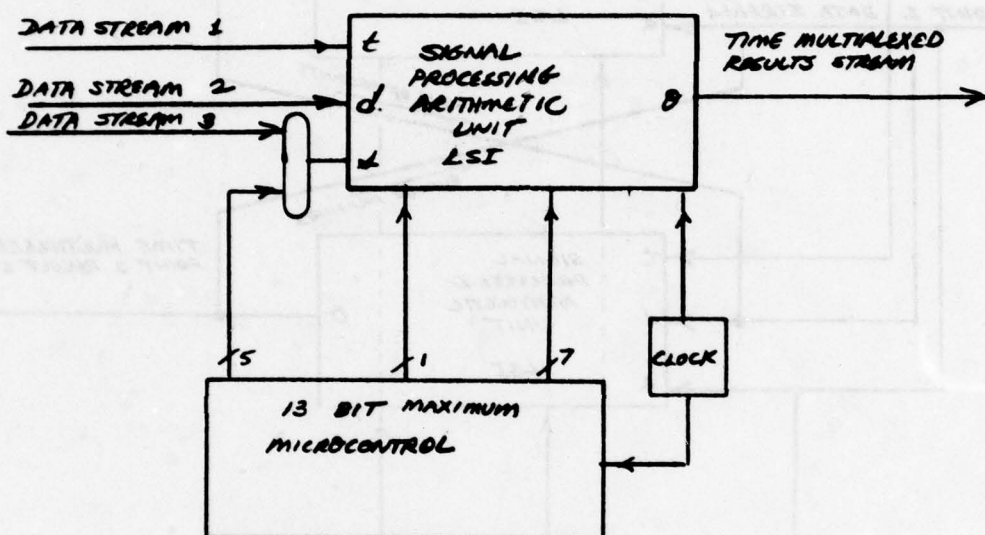
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DESCRIPTION

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ENGINEERING SKETCH

ORIGINATOR

DATE

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SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

Figure 10
Complex Arithmetic Microprocessor
Block Diagram

SIZE

A

CODE IDENT NO.

11982

SK

MJO

SCALE

165

SHEET 1 OF

SK		REVISIONS		
LTR	DESCRIPTION	DATE	APPROVED	
ENGINEERING SKETCH		Figure 11 TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR	DATE	Sequential Mode FFT Butterfly or Kernel Processor Block Diagram		
		SIZE A	CODE IDENT NO. 11982	SK
MJO		SCALE 166		SHEET 1 OF

SK

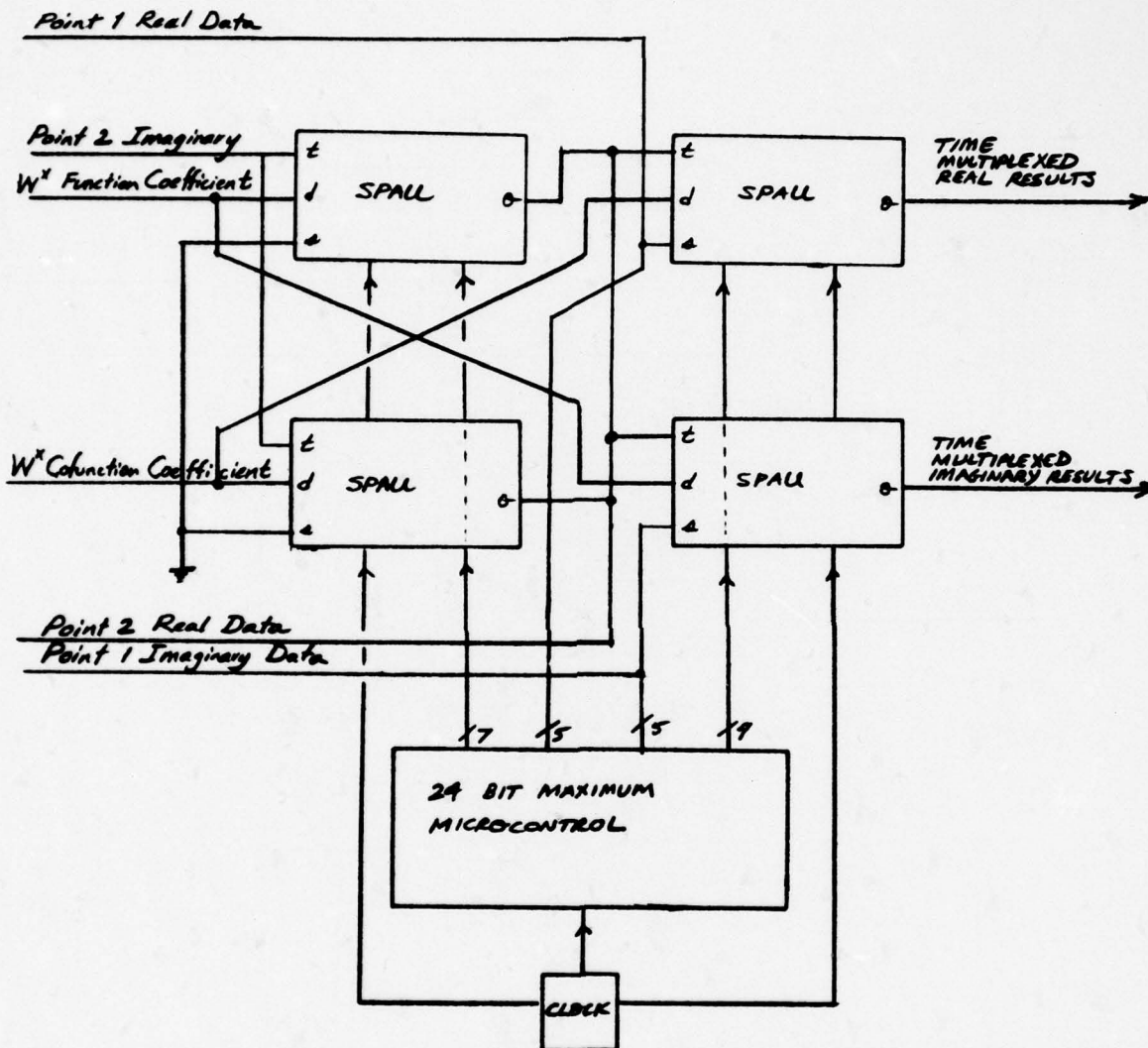
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Figure 12

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

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DATE

Pipeline Mode
FFT Butterfly or Kernel Processor
Block Diagram

SIZE

CODE IDENT NO.

A

11982

SK

MJO

SCALE 167

SHEET 1 OF

APPENDIX B

DETAILED LAYOUT AND CIRCUIT DESIGN OF SPAU 1

Due to its complexity and the many disjoint functions incorporated into the SPAU 1 design, the layout of this chip represented a formidable challenge. The basic technology employed, the triple diffusion process, also has a restriction to use only single level of metallization for both power and signal bus. Although TRW maintains and is developing a CAD effort in LSI, it was clear that none of these were sufficiently advanced to handle a problem of the magnitude offered by the SPAU 1. The SPAU 1 called for a custom layout design; however, certain standardizations were employed which reduced the manual task and a maximum use was made of computer-designer interactive aids, the Applicon system.

Standardization was used in the size of the circuit cell and the power bus interface with these cells. The circuit cell is rectangular with signal entry and exit on all four sides. This facilitated the two dimensional multiplier block of logic, the largest electronic segment on the chip. Figure

2 shows the SPAU Layout Plan and the circuit cell dimensions used. The overall chip dimensions are 315 by 351 mils. In the list of figures included in Appendix B, the schematic diagram of all circuit cells are shown. Also shown in each cell is the approximate placement for all input and output signals and any routing of control lines through the cell.

The type of logic circuits used can be determined from the schematic diagrams. All inputs and outputs are TTL logic compatible, but not necessarily identical as can be determined from a review of the SPAU Specification. The EFL (emitter follower logic) is most often used, but other logic forms are used where there are circuit reasons for doing so. EFL is used in the D and T registers and extensively in the multiplier array. The multiplier array uses non-threshold AND-OR gates without level restoration through the entire array. At each one bit product point in the array both true and complement output signals for both carry and sum outputs are fully implemented (so called dual railing). The final dual rail outputs are compared via a differential amplifier which leads quite fortuitously into CML (current mode logic) logic. The product register R is consequently implemented with CML circuits and level restored to EFL levels by a Norton mirror circuit (see Cell R and Cell X).

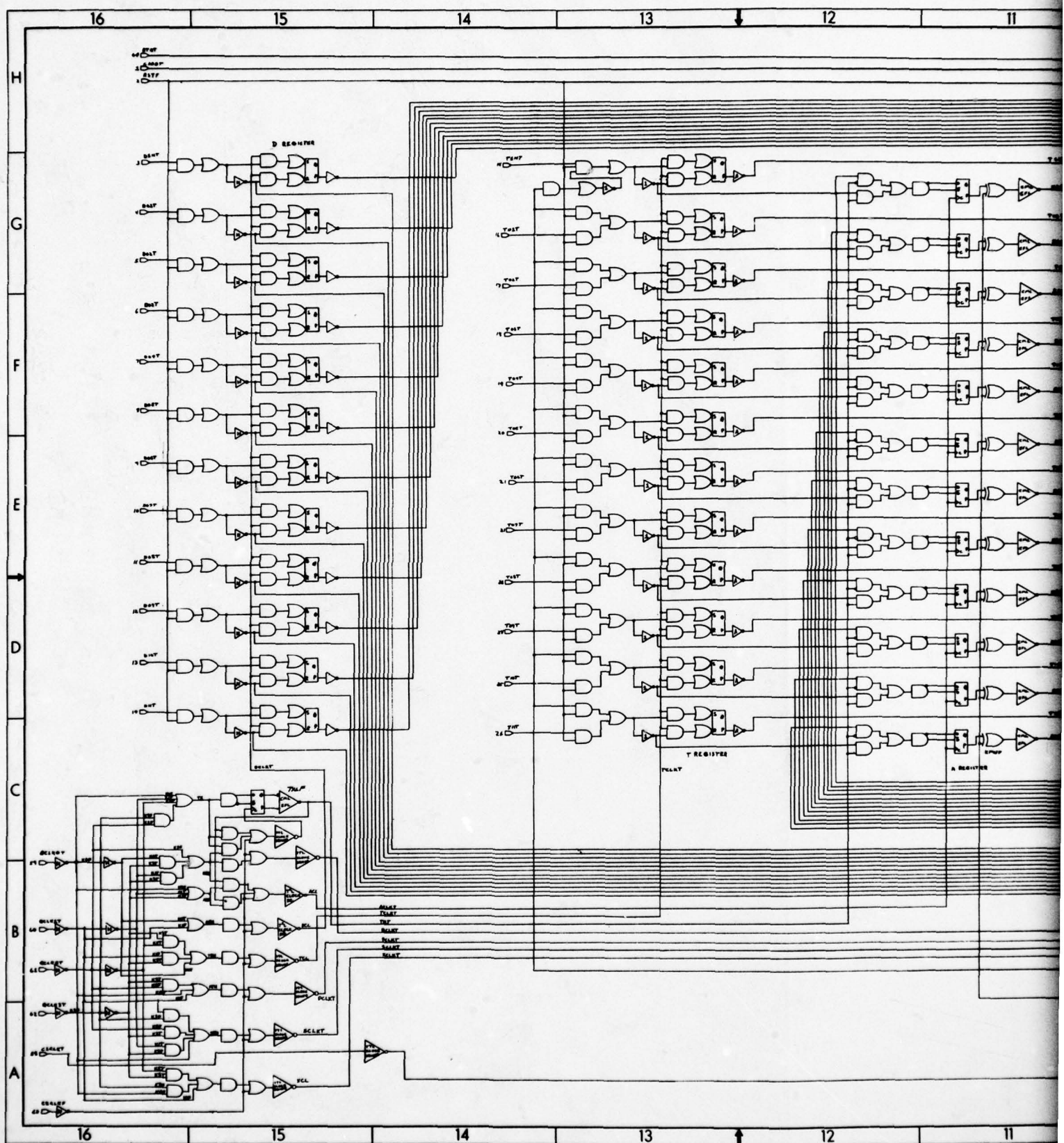
In the figures of the circuit cells, at the upper right hand corner the number of devices used (a device is a transistor, resistor, or diode) and the average power consumption in milliwatts. The spatial distribution of power is shown in Figure 3 and the device count in Figure 4. These are respectively 5 watts (nominal, 25°C) and 13,796 devices for the SPAU. Power bus current, thermal interface, diffusion parameters, and package connections are shown in Figures 5 through 9, respectively. This is followed literally by Cells A through Z in the figures of this Appendix.

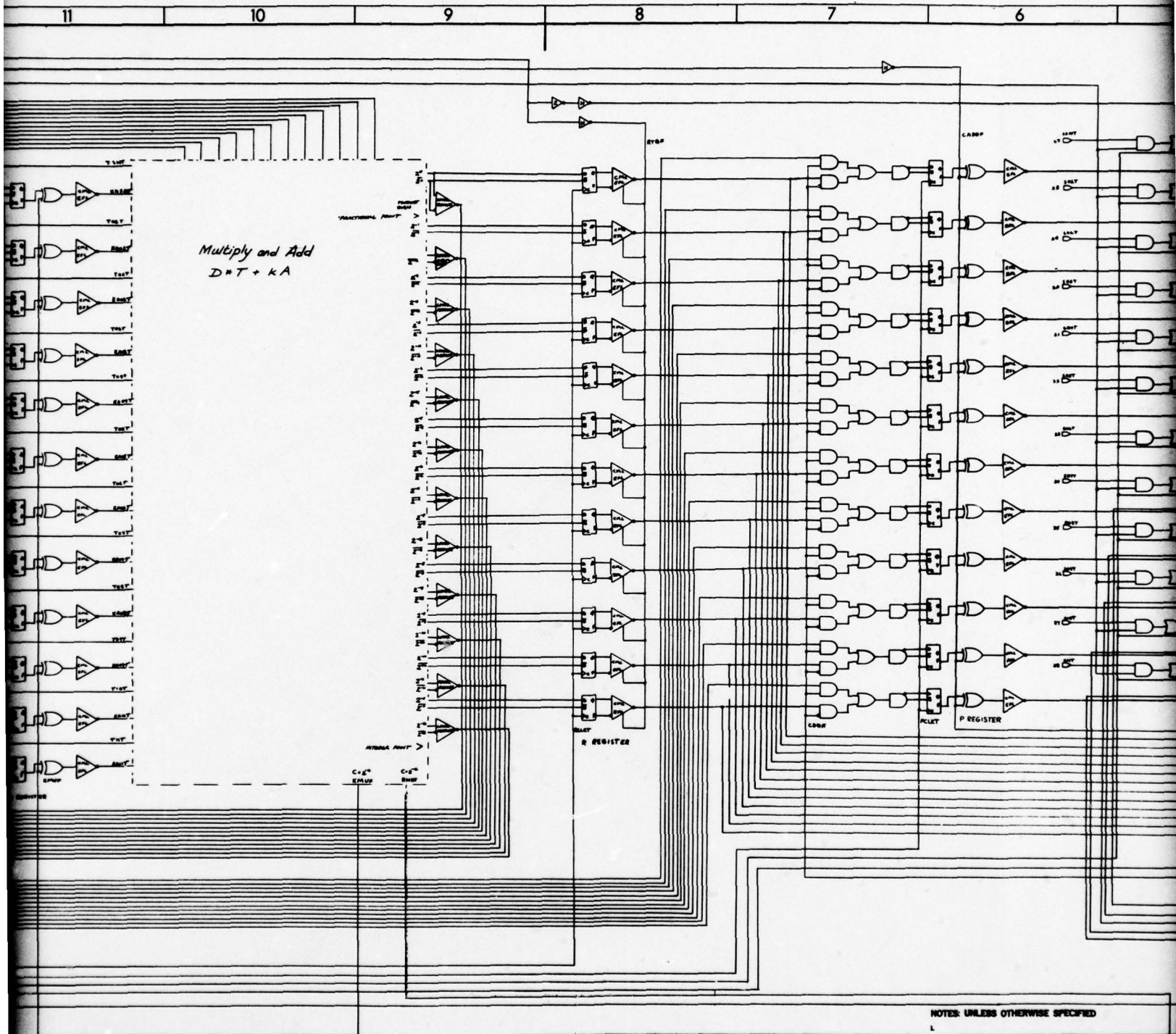
LIST OF FIGURES - SPAU 1, APPENDIX B

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1	LSI Implementation Arithmetic Unit Logic Schematic	26
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16	CELLAXD	41
17	CELLAXF	42
18	CELLCAD	43
19	CELLCDB	44
20	CELLCX	45
21	CELLC1C	46
22	CELLC2C	47
23	CELLD	48
24	CELLDCK	49
25	CELLDCL	50
26	CELLDCR	51
27	CELLDE	52
28	CELLDX	53
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35	CELLLRP	

LIST OF FIGURES - SPAU1(cont'd)

<u>FIGURE</u>	<u>TITLE</u>	<u>FIGURE</u>	<u>TITLE</u>
36	CELLSX	69	Overflow Control CKT
37	CELLNE	70	CELLUOC
38	Limiter Control Logic	71	CELLX
39	CELLLMC	72	CELLXCL
40	CELLO	73	CELLZ
41	CELLOSN	74	STD TRANSISTOR MODELS
42	CML D Type F/F with EX. OR Gate & Restorer	75	COMPONENT CMLX
43	CELLPCL	76	COMPONENT CML
44	CELLPP	77	BIT SLICE
45	CELLQC0		
46	CELLQC1		
47	CELLQC2		
48	CELLQC3		
49	CML D Type FF CELLR		
50	CELLRCL		
51	CELLRND		
52	CELLRTB		
53	CELLRX		
54	CELLS		
55	CELLSB		
56	CELLSCA		
57	CELLSCC		
58	CELLSCL		
59	CELLSNC		
60	CELLSX		
61	CELLSXL		
62	CELLT		
63	CELLTCL		
64	CELLTX		
65	CELLTXI		
66	CELLTXL		
67	CELLU		
68	CELLUA		





11002 FRAME

2

SK

Q, Q, = -8400, 9408

R	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
1	PW END	log	log	th	den	den	den	den	den	den	den	den	den	den	den	den	den	PW +100	-8624
2		NW1	NW2	DCL	DE	DCK	DCR	D	D	D	D	D	D	D	D	D	NE	den	7840
3		T	A	AA	CX	FX	FX	FX	FX	FX	FX	FX	FX	FX	FX	FX	U		7056
4		T	A	AA	CX	AX	AX	RX	RX	RX	RX	RX	RX	RX	RX	RX	U		6272
5		T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	ALL OUTLINE BEHIND IN PAGES	5488
6	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U		4704
7	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	3920
8	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	3136
9	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	2352
10	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	1568
11	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	784
12	log	T	A	AA	CX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	AX	U	den	--- 0
13	log	T	A	AA	CXE	AXD	AXD	AXD	AXD	AXD	AXD	AXD	AXD	AXD	AXD	AXD	U	den	-784
14	den	TS	A	AU	EX	DX	DX	DX	DX	DX	DX	DX	DX	DX	DX	DX	RND	den	-1568
15	PW END	TEL	TXL	UA	SXM	SX	SX	SX	SX	SX	SX	SX	SX	SX	SX	SXL	KMU	den	-2352
16		ACL	(TXL)	REL	R	R	R	R	R	R	R	R	R	R	R	R	R	PW +100	-3136
17	RSR	LDI	(EAT)	(BLI)	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	PP	CDB		-3920
18	Q0	Q00	(LRP)	PCL	P	P	P	P	P	P	P	P	P	P	P	P	CAD	den	-4704
19	Q1	Q01	(WOC)	LMC	ADS	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	AD	RTB	den	-5488
20	Q2	Q02	(SCC)	XCL	XS	X	X	X	X	X	X	X	X	X	X	X	EST	den	-6272
21	Q3	Q03	(LSX)	SCL	S	S	S	S	S	S	S	SNC	SNC	SNC	SNC	SNC	SB	den	-7056
22	Q4	(SW)	(SW2)	CZC	CEN	O	O	O	O	O	O	O	O	O	O	O	SCA	den	-7840
23	PW +100			Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	Q04	den	PW END	-8624

7500 6720 5880 5040 4200 3360 2520 1680 840 0 840 1680 2520 3360 4200 5040 5880 6720

APPLICON
COORDINATE

SK

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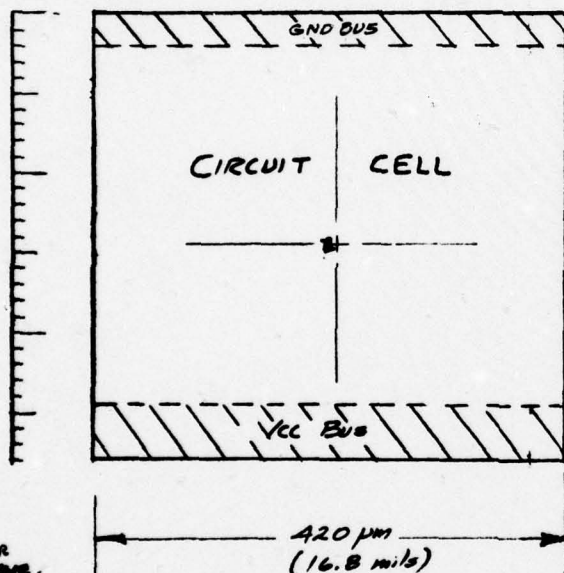
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GRID UNITS (G.U. = 28 DAU)

392 μm
(15.68 mils)CELL AREA 164,640 μm²
(263.4 mils²)Approx device density
4.2 mils²/device

CHIP SIZE

$$315 \times 351 = 1.1057 \times 10^5 \text{ mils}^2$$

ESTIMATED CHIP YIELD = 24.6% (@ D₀ = 2.5 defects/cm²); $Y = (1 + D_0)^{-3}$

No. of chips per 2" WAFER = 19.7

WAFER YIELD = 4.9

CHIP COST (@ 22¢/wafer) = 25.51

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

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DATE

SPAU LAYOUT PLAN

12 BIT WORD LENGTH

SIZE

CODE IDENT NO.

B

11982

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Figure 2

SCALE

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SYSTEMS 3663/REV. 12-71

2

SK

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C	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
1																						
2																						
3																						
4																						
5																						
6																						
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22																						
23																						
24																						
25																						
26																						
27																						

No. listed are in units of milliwatts

12 WIDE SPAU	12 WIDE SPAU	12 WIDE SPAU	12 WIDE SPAU
Row	12	12	12
1	278	85	
2	169	34	
3	182	36	
4	198	40	
5	198	40	
6	198	40	
7	198	40	
8	198	40	
9	198	40	
10	198	40	
11	198	40	
12	198	40	
13	198	40	
14	207	41	
15	166	33	
16	370	74	
17	252	51	
18	398	112	
19	242	48	
20	472	94	
21	282	56	
22	177	35	
23			
24			
25			
26			
27			
TOTAL	5140	1028	
MIN			
MAX			

ENGINEERING SKETCH

ORIGINATOR

DATE

JB

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2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

POWER DISTRIBUTION 12 WIDE SPAU

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 3

SCALE

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SYSTEMS DES REV. 12-71

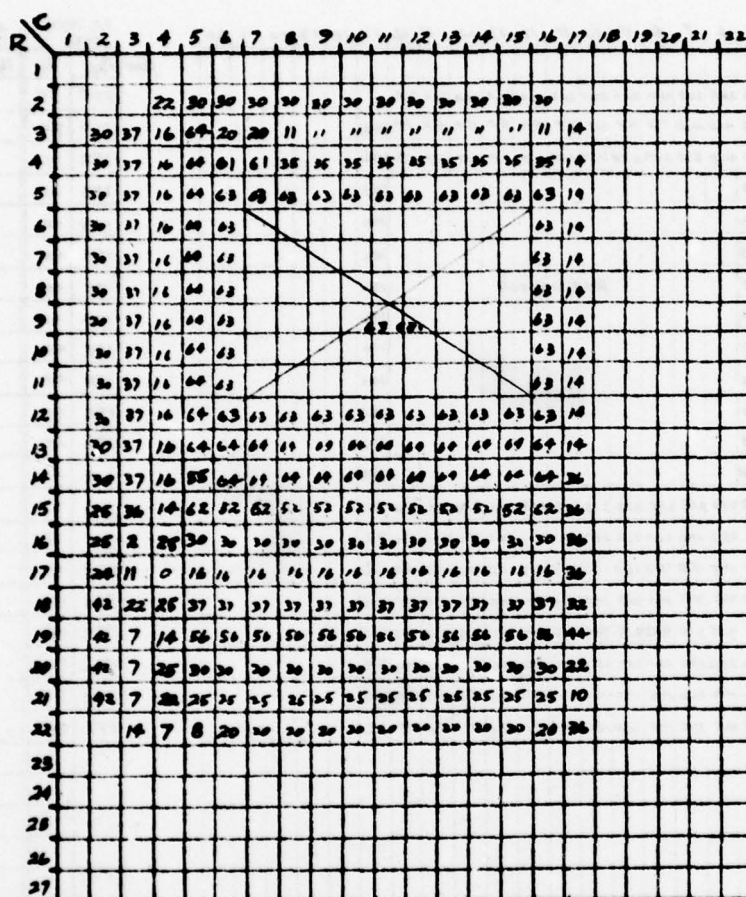
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DATE _____

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No. of Deaths Per 1000	Percentage
362	.72
300	.56
598	.30
864	.23
884	.28
854	.23
830	.23
854	.23
854	.23
850	.23
804	.23
868	.23
878	.24
755	.22
448	.83
263	.98
565	.99
779	.31
456	1.04
381	.74
205	.62

TOTAL 13,726

DOWNED

0.37 mm/ounce
Avg.

CHIP SIZE

302 x 360 miks

7.9 mils²/Dance

ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR <i>J.B.</i>	DATE	<u>DEVICE COUNT</u>	
		12 BIT WIDE SPAU	
		SIZE A	CODE IDENT NO. 11982
		SK	Figure 4
MJO 2349-71		SCALE 178	SHEET 1 OF

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

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ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR JIB	DATE	VCC2 BUS CURRENT DISTRIBUTION SPA4	
		SIZE A	CODE IDENT NO. 11982
		SK Figure 5	
MJO 2349-71		SCALE 179	SHEET 1 OF

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE _____

VCC2 BUS CURRENT DISTRIBUTION
SPAU

SIZE

CODE IDENT NO.

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Figure 5

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2349-71

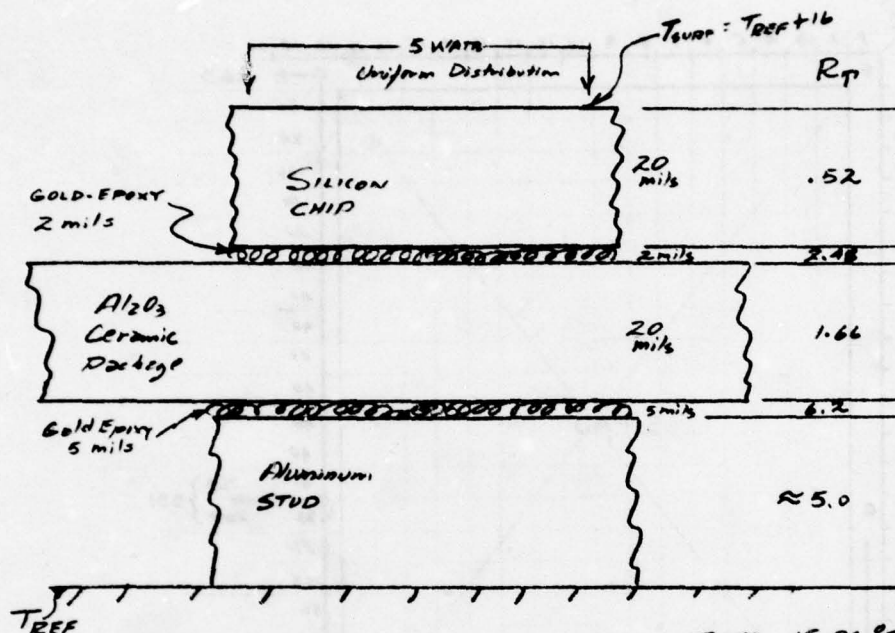
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	R_p
SILICON:	170 (°C/mil) / (WATTS/mil ²)
AU-EPXY:	2.23×10^{-4} "
Al ₂ O ₃ :	1500 "
CU:	103 "

Measured thermal resistance
4.5°C/WATT 8/5/75

ENGINEERING SKETCH		TRW SYSTEMS GROUP	
ORIGINATOR JIB		ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
DATE		SPAU THERMAL INTERFACE	
MJO		SIZE A	CODE IDENT NO. 11982
		SK FIGURE 6	
		SCALE 180	SHEET 1 OF

SK

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DIFFUSION PARAMETERS FOR SPAU CHIP

Triple 2 and Semi were interrogated for processing parameters appropriate for the SPAU design. The principal device characteristics sought are

1. Pinched collector sheet resistance, $R_{scp} = 1000 \Omega/\square$
2. Alpha cut-off freq. npn, $f_{an} = 250 \text{ MHz}$
3. Alpha cut-off freq. pnp, $f_{ap} = 70 \text{ MHz}$
4. Unpinched collector sheet resistance, $R_{sc} = 150 \Omega/\square$

TABLE I shows the results

SUB-STRATE	R_{so}	X_{jc}	X_{jb}	X_{je}	R_{scp}	R_{sc}	f_{an}	f_{ap}	REMARKS
$\Omega\text{-CM}$	Ω/\square	μm	μm	μm	Ω/\square	Ω/\square	MHz	MHz	$R_{sc} = 150 \Omega/\square$; $R_{sc} = 74 \Omega/\square$
.8	150	4.8	2.5	1.8	1070	10.8K	123	69	
.8	150	5.2	2.3	1.5	670	4.9K	82	45	
.8	150	4.5	2.0	1.5	710	17K	208	57	
.8	150	4.5	2.2	1.7	906	24K	248	67	
1.2	150	4.5	2.2	1.7	990	24K	265	71	
1.0	150	4.5	2.2	1.7	950	24K	258	69	
1.0	125	4.5	2.2	1.7	925	24K	251	69	
→ 1.0	138	4.3	2.2	1.7	1090	25K	258	81	$R_{sc} = 150$; $R_{sc} = 74 \Omega/\square$
SPEC 1.0 ± .2	120 ± 12	4.3 ± .1	2.2 ± .1	1.7 ± .05	1000 ± 100	25K ± 2K	250 ± 30	80 ± 15	$R_{sc} = 150 \pm 10$; $R_{sc} = 72$

Selected target processing values are shown in the last flagged entry.

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ORIGINATOR

DATE

J.B.

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIADIFFUSION PARAMETERS FOR
SPAU

SIZE

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Figure 7

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AD-A057 874

TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CALIF
LSI IMPLEMENTATION.(U)
DEC 77 J L BUIE

F/G 9/5

UNCLASSIFIED

AFAL-TR-77-261

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NL

3 of 4
AD
A057 874



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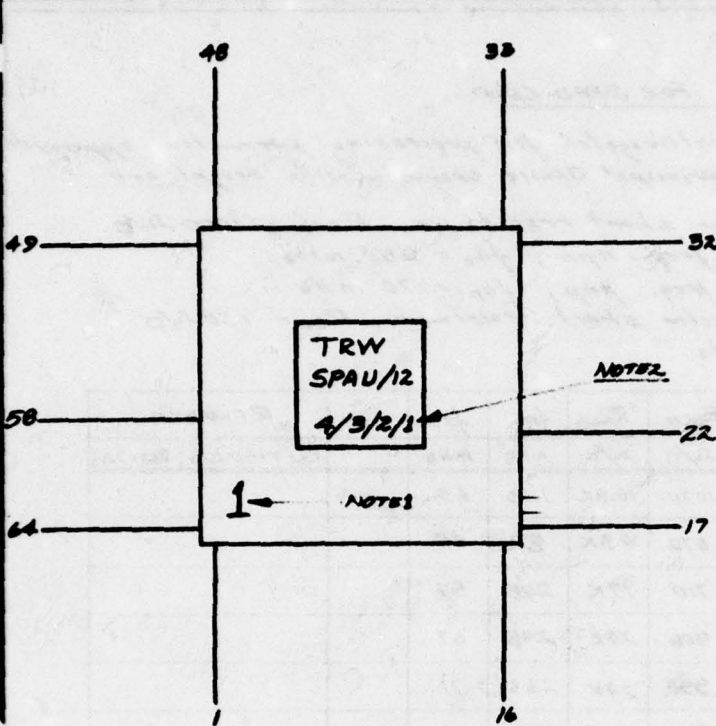
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TOP VIEW

64 LEAD FLAT PACKAGE
KOTO CERAMIC CO. LTD
KD-74043-A
(400 mil sq. die cavity)

NOTES:

1. TOP VIEW PIN INDEX NUMBER
2. UNIT IDENTIFICATION
1ST DIGIT: RUN NO.
2ND DIGIT: WAFER NO.
3RD DIGIT: ROW NO.
4TH DIGIT: COLUMN NO.

PIN#	SIGNAL	PIN#	SIGNAL
1	+Vcc	33	+Vcc
2	C2CLKF	34	D10
3	OSN	35	D9
4	O1	36	D8
5	O2	37	D7
6	O3	38	D6
7	O4	39	D5
8	O5	40	D4
9	O6	41	D3
10	O7	42	D2
11	O8	43	D1
12	O9	44	DSN
13	O10	45	T11
14	O11	46	T10
15	S11	47	T9
16	GND	48	GND
17	SSN	49	T8
18	S1	50	T7
19	C1CLKT	51	T6
20	RTBT	52	T5
21	CADDT	53	T4
22	+Vcc	54	T3
23	S2	55	T2
24	S3	56	T1
25	S4	57	TSN
26	S5	58	GND
27	S6	59	RSTF
28	S7	60	QCLK0T
29	S8	61	QCLK1T
30	S9	62	QCLK2T
31	S10	63	OCLK3T
32	D11	64	BZZT

ENGINEERING SKETCH

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TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SPAU/12 PACKAGE CONNECTIONS

SPAU

SIZE

CODE IDENT NO.

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Figure 8

SCALE

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SK

REVISIONS

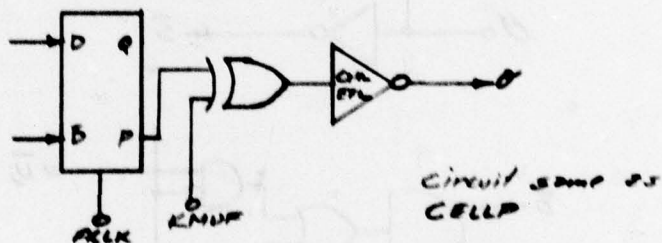
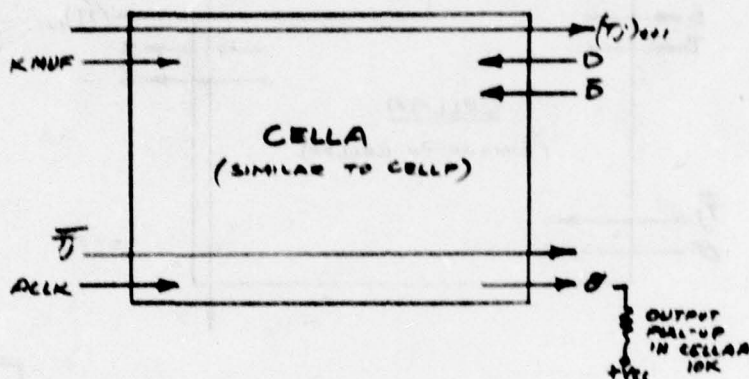
LTR

DESCRIPTION

DATE

APPROVED

34.4 mw.
57 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

J-1B

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLA

6PAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 9

SCALE

183

SHEET 1 OF

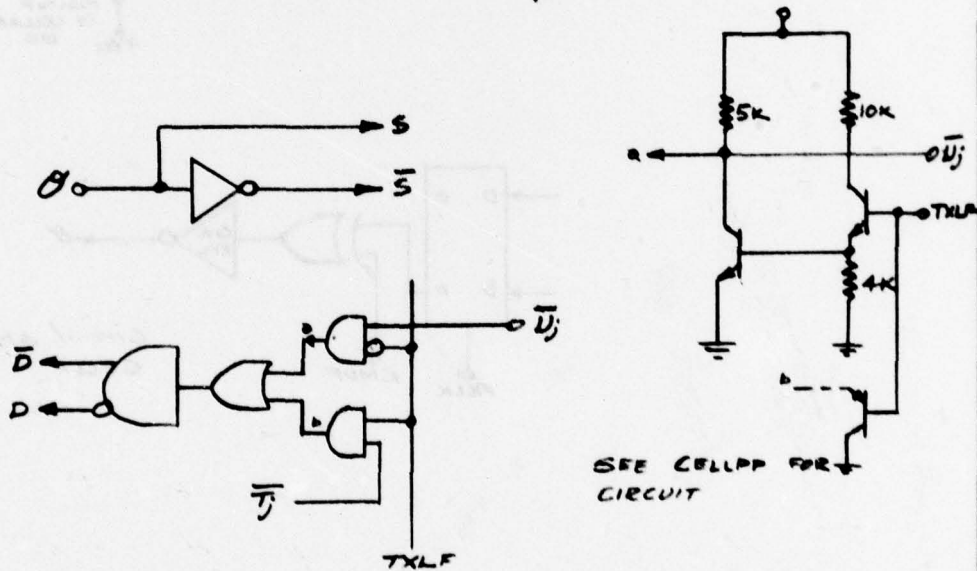
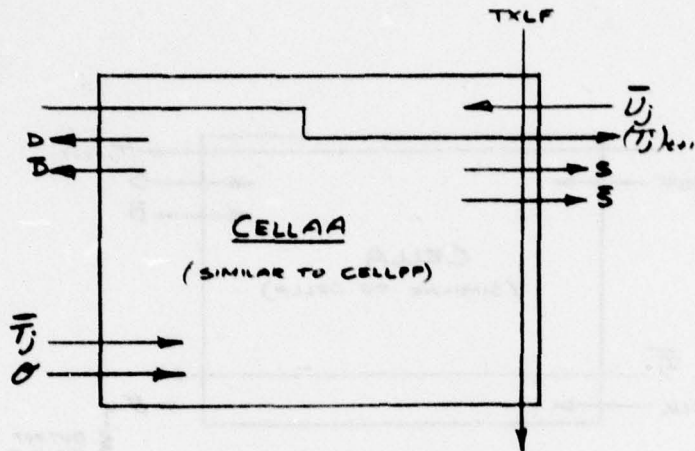
SYSTEMS 883 REV. 12/71

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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15.8 MW,
16 Devices



ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLAA	
MJB		SPA	
SIZE	CODE IDENT NO.	SK	Figure 10
A	11982		
MJO	2349-71	SCALE 184	SHEET 1 OF

SK

REVISIONS

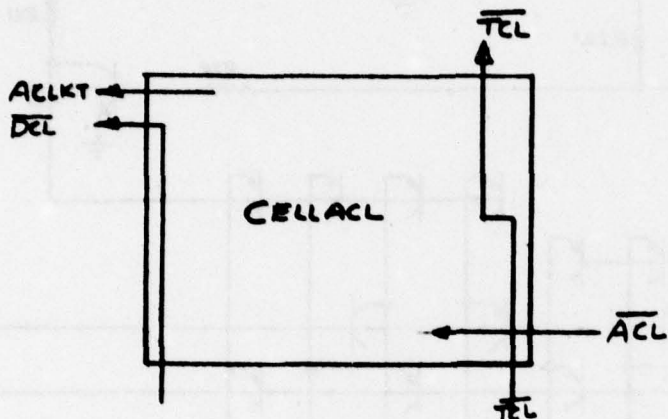
LTR

DESCRIPTION

DATE

APPROVED

37.7 MW.
25 Dealers



SAME AS XCL
EXCEPT FOR BUSING

ENGINEERING SKETCH

ORIGINATOR

DATE

JMB

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLACL

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 11

MJO

2349-71

SCALE

185

SHEET 1 OF

SK

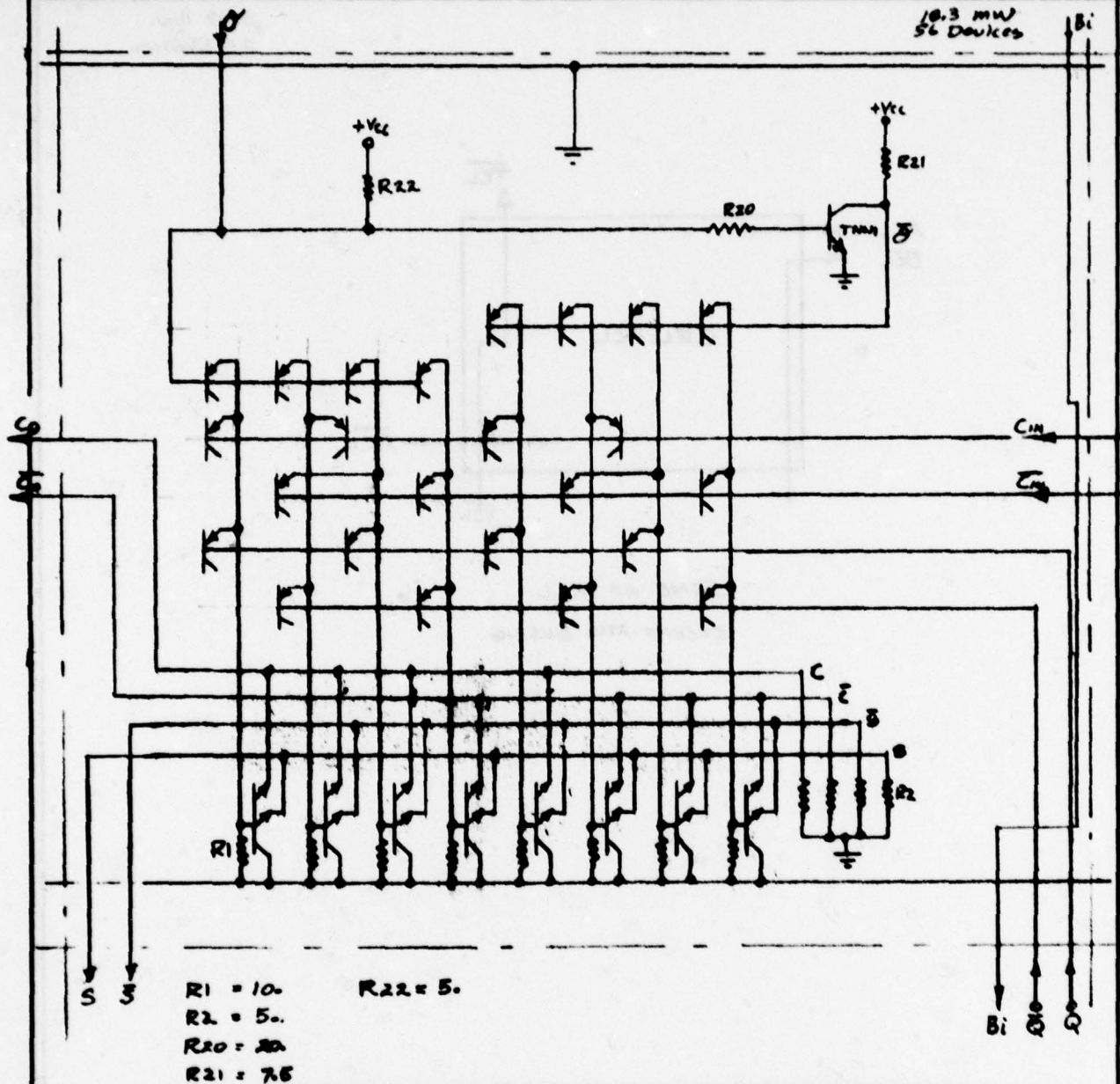
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

10.3 MW
56 Devices

ENGINEERING SKETCH

ORIGINATOR

DATE

J.B.

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLAD

SPA U

SIZE

A

CODE IDENT NO.

11982

SK

Figure 12

SCALE

186

SHEET 1 OF

SYSTEMS 623 REV. 12-71

SK

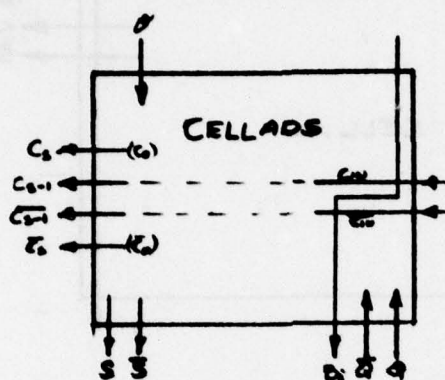
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



EDIT FROM CELLAD
FOR C_{s-1} & E_{s-1} OUTPUTS
ON LEFT

ENGINEERING SKETCH

ORIGINATOR

JLB

DATE

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLADS

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 13

MJO

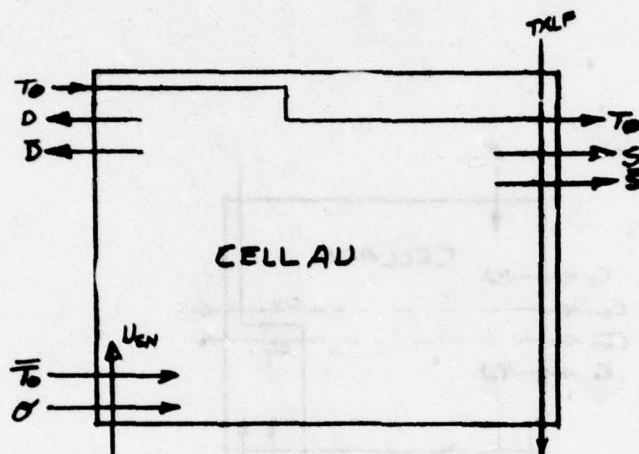
2349-71

SCALE 187

SHEET 1 OF

SK	REVISIONS		
	LTR	DESCRIPTION	DATE APPROVED

15.8 MW
16 Devices



SIMILAR TO CELLAA
BUT FOR BUSING

ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLAU	
JLB			
		SIZE	CODE IDENT NO.
		A	11982
MJO 2349-71		SK	Figure 14
		SCALE 100	SHEET 1 OF

SK		REVISIONS		
LTR	DESCRIPTION	DATE	APPROVED	
<p> T1-T26 = MODEL TP1 T27-T29 = MODEL TN1 T30-T37 = MODEL TN11 R1 = 20. R3 = 20. R5 = 10. R7 = 40. R2 = 10. R4 = 4. R6 = 10. R8 = 15. </p>				
<p> *CELLAXP USED ONLY AT INTERFACE WITH CELL PNC. NAME SPACE ADJUSTMENT. </p>				
ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR	DATE	CELLAX (CELLAXP)		
MB		SPRU		
SIZE	CODE IDENT NO.	<div style="display: flex; justify-content: space-between; align-items: center;"> SK Figure 15 </div>		
A	11982			
SCALE		189	SHEET 1 OF	
2349-71				

SK

REVISIONS

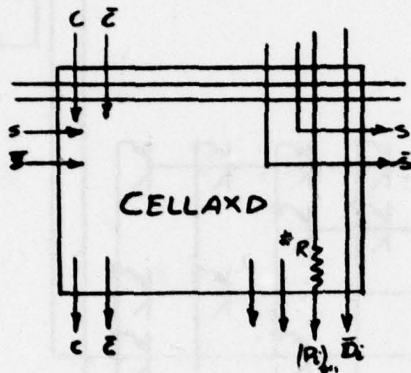
LTR

DESCRIPTION

DATE

APPROVED

8.58 MW.
64 Devices



* Same as CELLAX EXCEPT
for resistor placed in
(Di)_n load.

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

J. B. Bini

CELLAXD

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 16

MJO

SCALE

190

SHEET 1 OF

SK

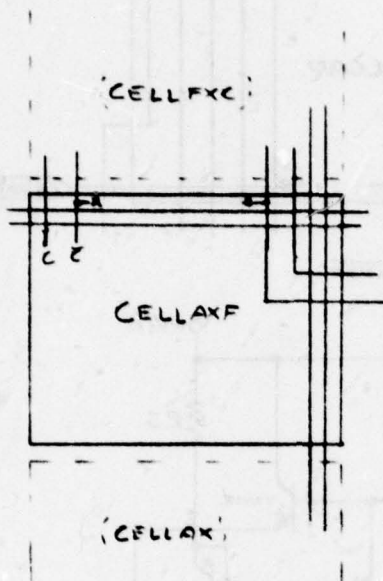
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

8.50 MW.
61 DEVICESCELLAXF IS IDENTICAL
TO CELLAX EXCEPT FOR
REMOVAL OF PULLDOWN
RESISTORS ON C & E
INPUTS *.

ENGINEERING SKETCH

ORIGINATOR

J. B.

DATE

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLAXF

SPAN

SIZE

A

CODE IDENT NO.

11982

SK

Figure 17

MJO

SCALE

191

SHEET 1 OF

SYSTEMS 523 REV. 12-71

SK

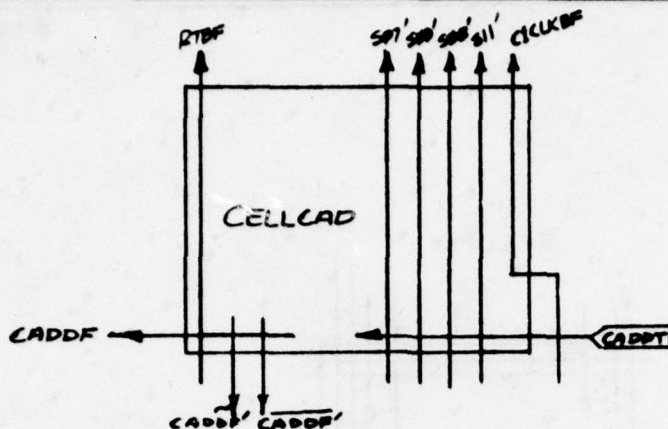
REVISIONS

LTR

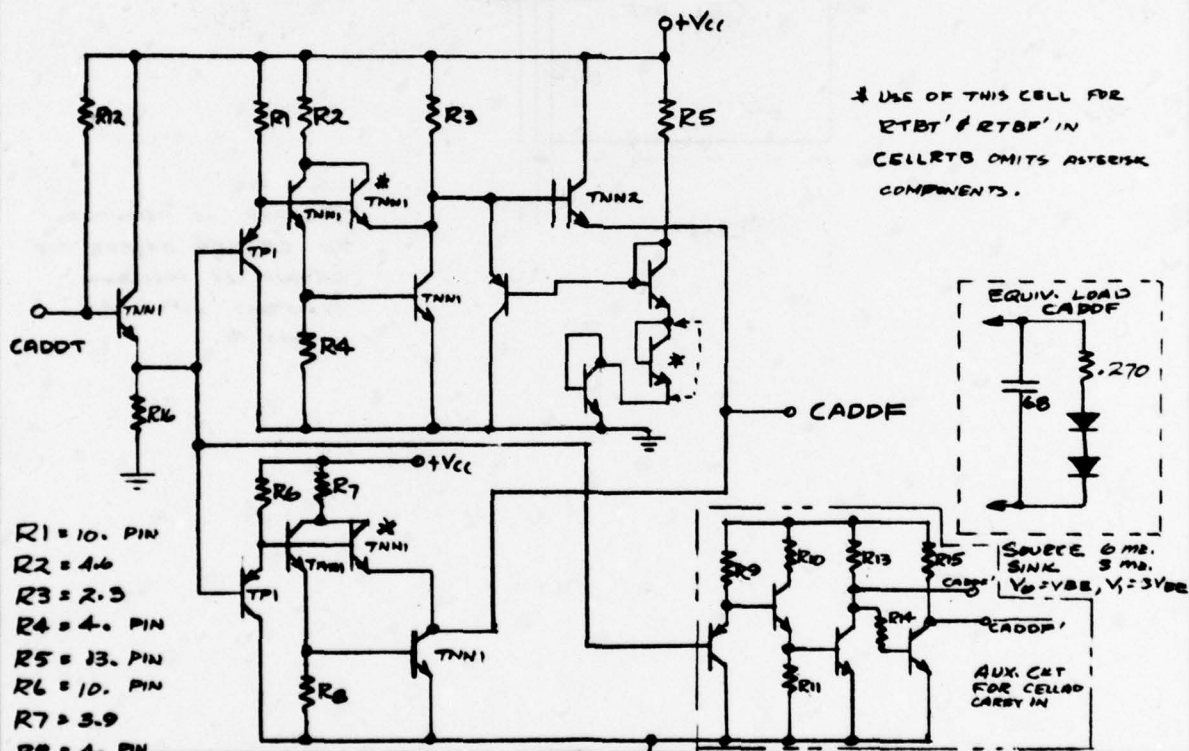
DESCRIPTION

DATE

APPROVED



26-5 MW.
32 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLCAD

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 18

SCALE

192

SHEET 1 OF

SYSTEMS 823 REV. 12-71

SK

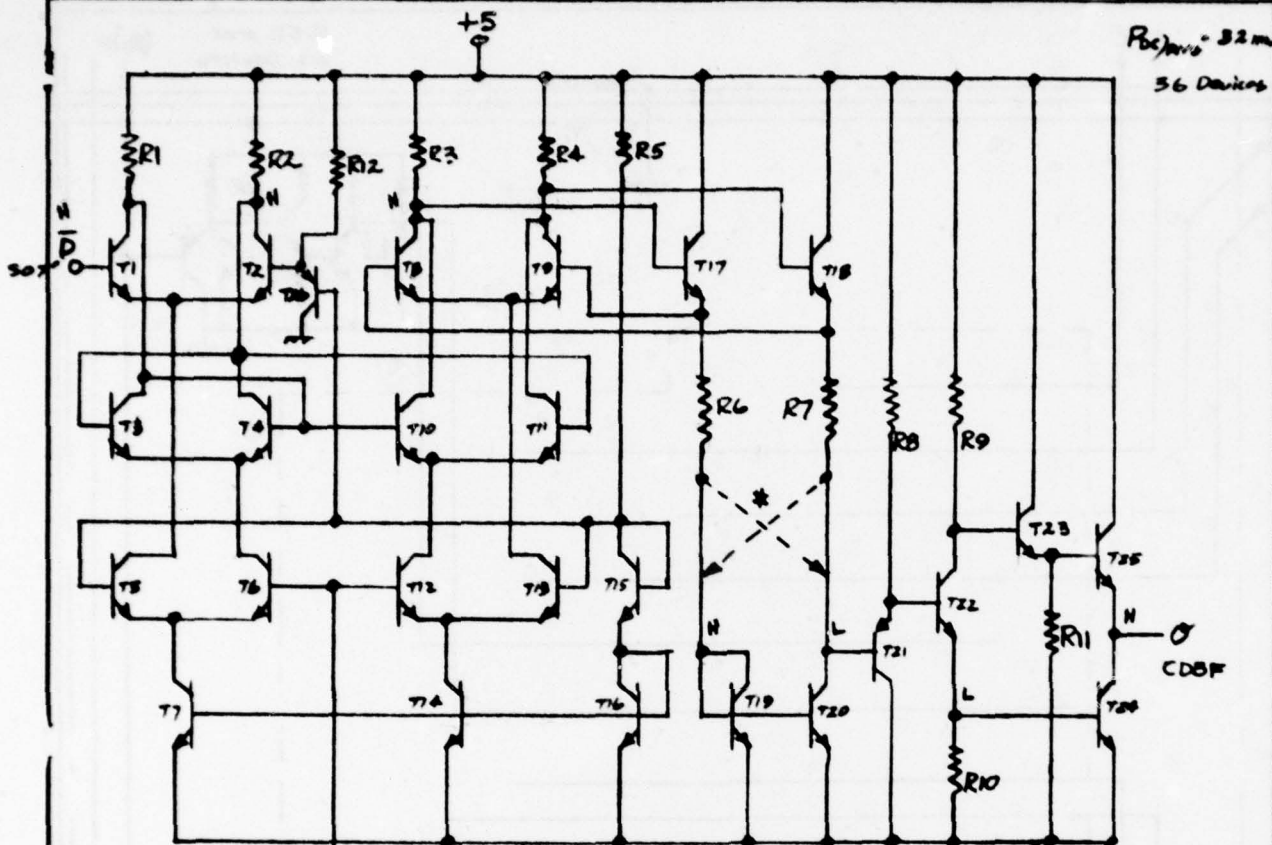
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



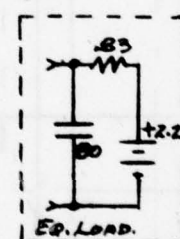
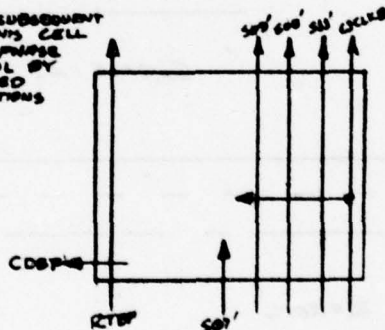
$P_{CE(max)} = 32m$
36 Devices

NOTE: ON SUBSEQUENT
USE OF THIS CELL
OUTPUT PHASE
REVERSAL BY
EXCHANGED
TERMINATIONS

T7, 10, 16, = MODEL TMS
T1, 2, 3, 4, 8, 9, 10, 11 = MODEL CML
T21 = MODEL TPA
ALL OTHERS = MODEL TMS

R1 = .75 R6 = 2. R11 = 20.
R2 = .75 R7 = 2. R12 = 9
R3 = 1.25 R8 = 10.
R4 = 1.25 R9 = 2.8
R5 = 2.75 R10 = 4.0

ALL R'S UNPINCHED EXCEPT R8, R10, R11



SINK > 5.0 mA.
SOURCE > 2.5 mA.
 $V_D = 1.5V, V_1 > 2.4$

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELL CDB

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 19

MJO

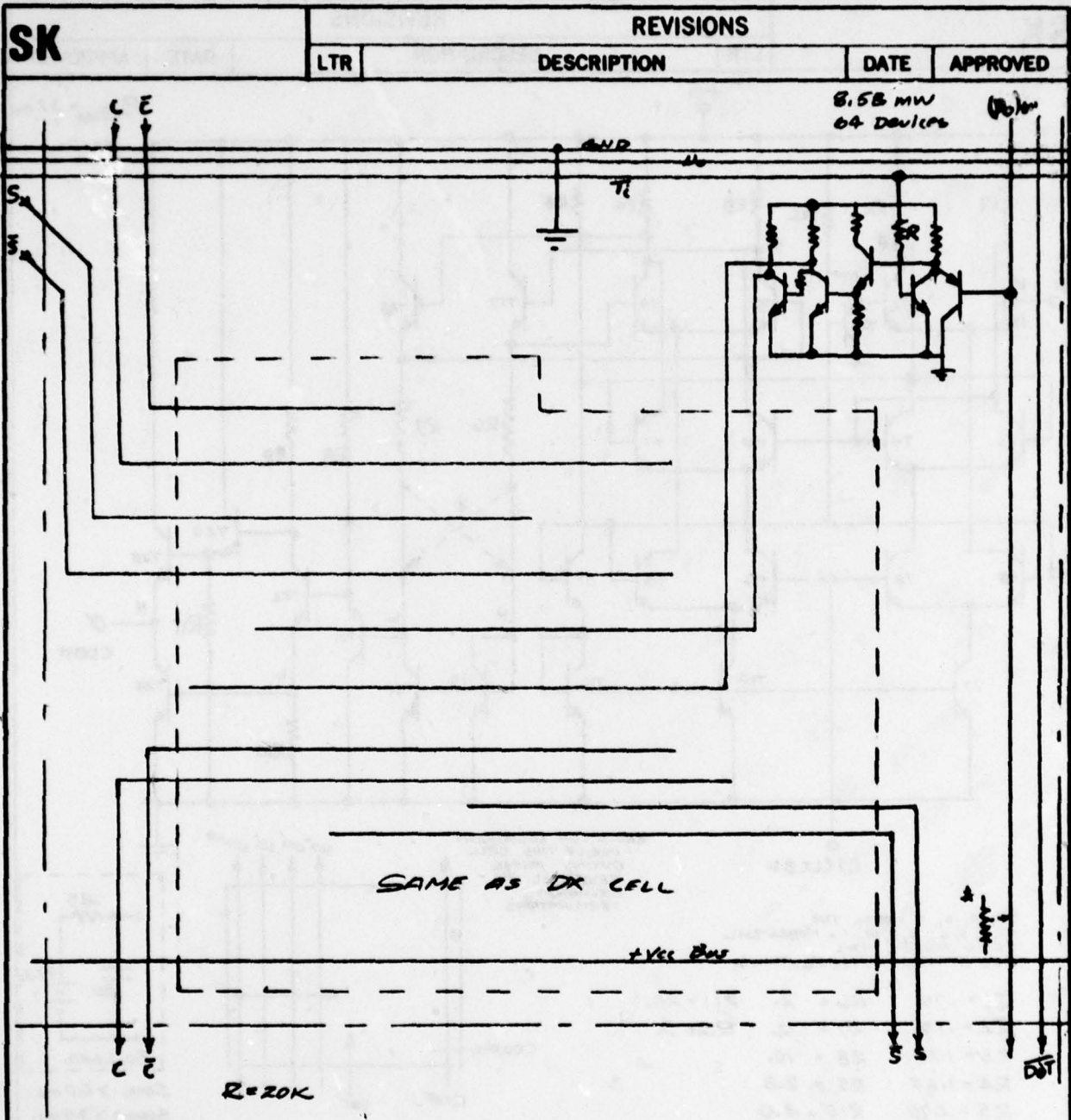
2349-71

SCALE

193

SHEET 1 OF

SYSTEMS DES REV. 10-71



*CELLCX
IS SAME AS
CELLCX DESPT
FOR ROUTING
PLAID IN
(DET), line.

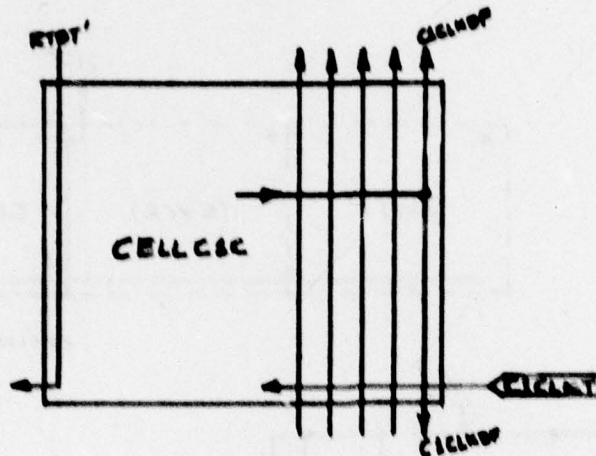
ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLCX (*CELLCX)	
JIB			
		SIZE	CODE IDENT NO.
		A	11982
		SK	Figure 20
MJO		SCALE	SHEET 1 OF
		194	

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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21.3 REV.
22.0 REV.



SIMILAR TO CELLCSK
EXCEPT FOR BUSING

ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLCSK	
JMB		SPAU	
SIZE	CODE IDENT NO.	SK Figure 21	
A	11982		
SCALE	195	SHEET 1 OF	
2349-71			

SK

REVISIONS

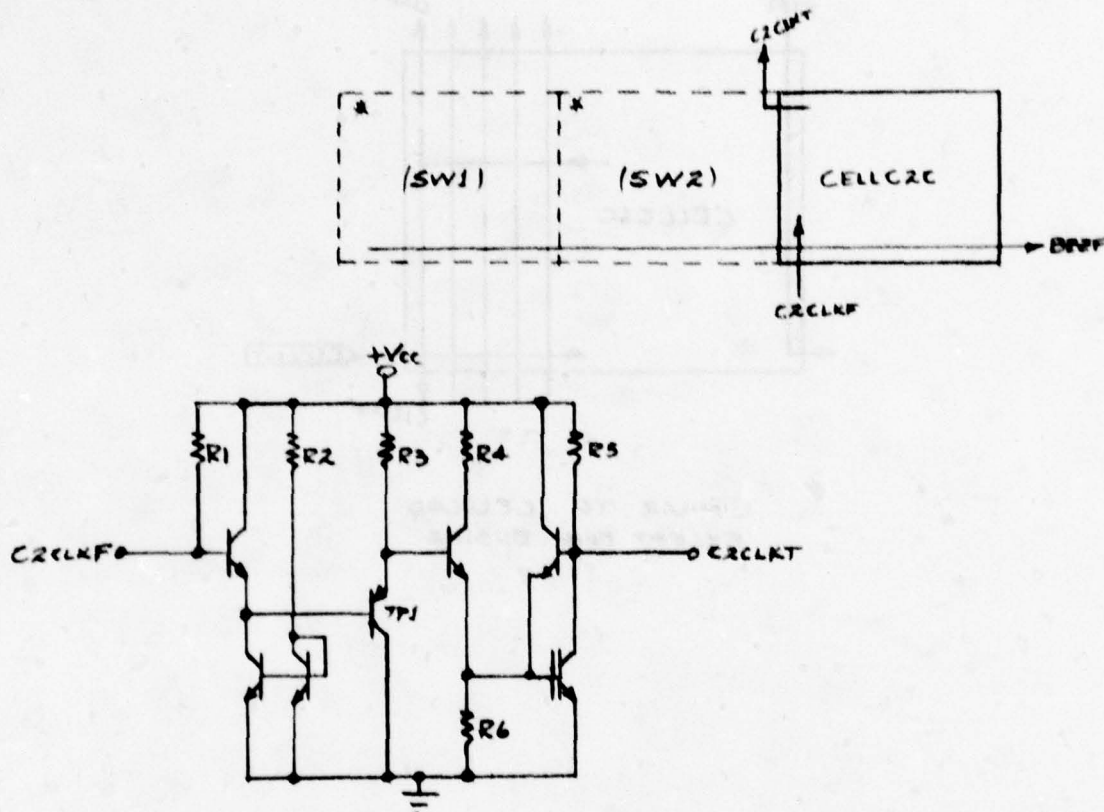
LTR

DESCRIPTION

DATE

APPROVED

*P_{DC} = 27.4 mW.
14 DOWNS.*



ALL NPNS MODEL TRANS

R1 = 50.

R5 = 1.6

R2 = 15.

R6 = 3.

R3 = 5.

R4 = 2.3

I_{SINK} 4.9 mA.

I_{SOURCE} 2.0 mA.

** Cells SW1 and SW2 are
included in the definition of
CELLC2C. 3/17/75*

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLC2C

SP4U

SIZE

CODE IDENT NO.

A

11982

SK

Figure 22

MJO

2349-71

SCALE

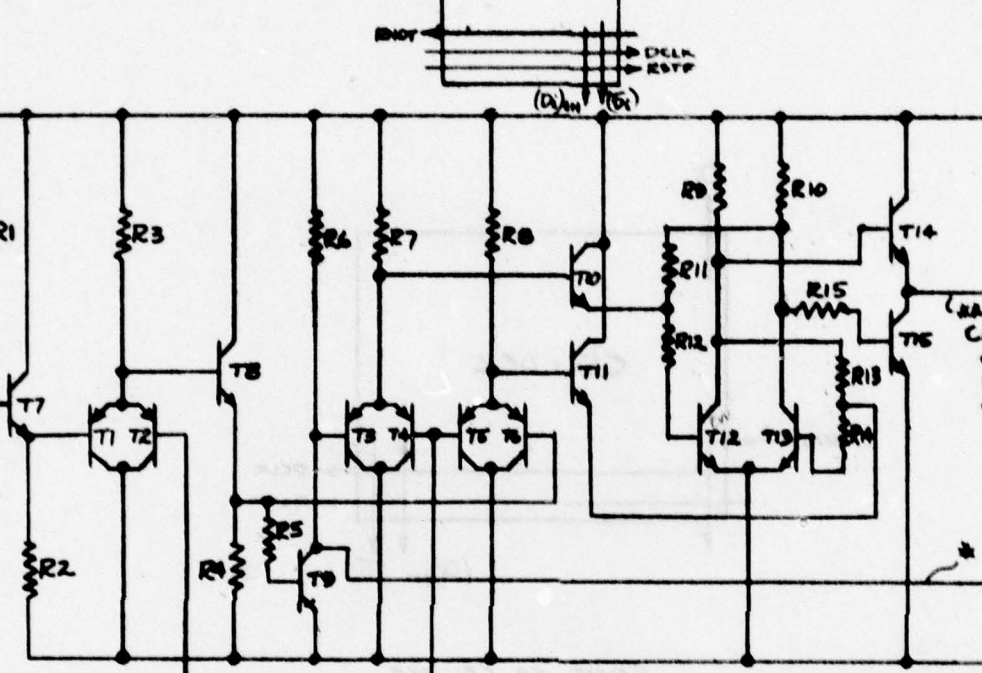
196

SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
		20.4 MW	30 DEVI 106



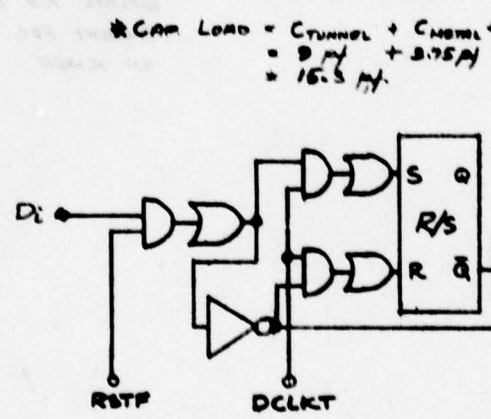
$(Di)_{out}$

20.4 MW
30 DEVI 106


CLAMP LOAD = $C_{TUNNEL} + C_{MOTEL} + C_{CODE}$
 $= 9 \mu F + 3.75 \mu F + 2.6 \mu F$
 $= 15.3 \mu F$

T1 - T6 = MODEL TP1
T7 - T15 = MODEL TN1

R1 = 50.	R9 = 5.
R2 = 3.	R10 = 2.5
R3 = 10.	R11 = 9.
R4 = 4.	R12 = 1.
R5 = 3.	R13 = 9.
R6 = 4.	R14 = 1.
R7 = 10.	R15 = 10.
R8 = 10.	



ENGINEERING SKETCH	
ORIGINATOR	DATE
MB	
MJO 2349-71	



ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

<h3 style="margin: 0;">CELLD</h3> <p style="margin: 0;">SPA U</p>	
SIZE	CODE IDENT NO.
A	11982
<div style="display: flex; justify-content: space-around; align-items: center;"> SK Figure 23 </div>	
SCALE	SHEET 1 OF
197	

20.4 mW
30 devices

Clones

Cross = 8 pt
Cost = 4 pt
Cost = 30 pt
<hr/>
42 pt

* CAM LOAD = $C_{TUNNEL} + C_{NORMAL} + C_{COVER}$
 $= 9 \text{ ft} + 3.75 \text{ ft} + 2.6 \text{ ft}$
 $= 15.3 \text{ ft}$

T1 - T6 = MODEL TP1
T7 - T15 = MODEL TN1

R1 = 50.	R9 = 5.
R2 = 5.	R10 = 2.5
R3 = 10.	R11 = 9.
R4 = 4.	R12 = 1.
R5 = 3.	R13 = 9.
R6 = 4.	R14 = 1.
R7 = 10.	R15 = 10.
R8 = 10.	

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELL D
SPA U

SIZE A	CODE IDENT NO. 11982
------------------	--------------------------------

SK

Figure 23

SCALE 197

SHEET 1 OF

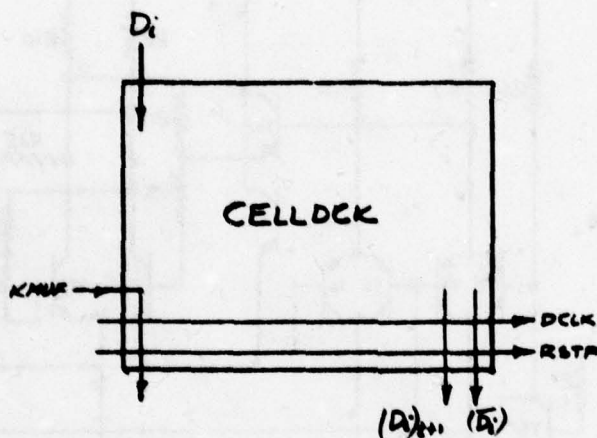
SYSTEMS DIV REV. 12-71

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------

20.4 MW.
50 DCLKs



SAME AS CELDER
EXCEPT FOR TERMINATION
OF KME

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JIB

CELLOCK

SIZE

CODE IDENT NO.

A

11982

SK

Figure 24

MJO

2349-71

SCALE

198

SHEET 1 OF

SK

REVISIONS

LTR

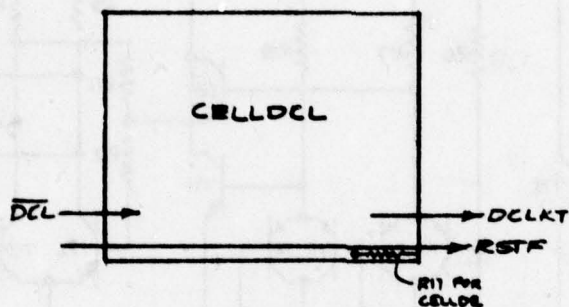
DESCRIPTION

DATE

APPROVED

29.7 MW.

22 Devices



SAME AS CELLSEL
EXCEPT FOR BUSING

ENGINEERING SKETCH

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLDCL

SIZE

A

CODE IDENT NO.

11982

SK

Figure 25

MJO

2349-71

SCALE

199

SHEET 1 OF

SYSTEMS 803 REV. 12-71

SK		REVISIONS																		
LTR	DESCRIPTION	DATE	APPROVED																	
20.4 mw. 30 Devices																				
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p> T1 - T6 = MODEL TP1 T7 - T15 = MODEL TNN1 </p> <table style="width: 100%;"> <tr> <td>R1 = 50.</td> <td>R9 = 5.</td> </tr> <tr> <td>R2 = 5.</td> <td>R10 = 2.5</td> </tr> <tr> <td>R3 = 10.</td> <td>R11 = 9.</td> </tr> <tr> <td>R4 = 4.</td> <td>R12 = 1.</td> </tr> <tr> <td>R5 = 3.</td> <td>R13 = 9.</td> </tr> <tr> <td>R6 = 4.</td> <td>R14 = 1.</td> </tr> <tr> <td>R7 = 10.</td> <td>R15 = 10.</td> </tr> <tr> <td>R8 = 10.</td> <td></td> </tr> </table> </div> <div style="width: 45%; text-align: center;"> </div> </div>					R1 = 50.	R9 = 5.	R2 = 5.	R10 = 2.5	R3 = 10.	R11 = 9.	R4 = 4.	R12 = 1.	R5 = 3.	R13 = 9.	R6 = 4.	R14 = 1.	R7 = 10.	R15 = 10.	R8 = 10.	
R1 = 50.	R9 = 5.																			
R2 = 5.	R10 = 2.5																			
R3 = 10.	R11 = 9.																			
R4 = 4.	R12 = 1.																			
R5 = 3.	R13 = 9.																			
R6 = 4.	R14 = 1.																			
R7 = 10.	R15 = 10.																			
R8 = 10.																				
ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA																		
ORIGINATOR 	DATE	CELLDCR SPAU																		
MJO 2349-71		SIZE A	CODE IDENT NO. 11982	SK																
SCALE 200		SHEET 1 OF																		
Figure 26 SYSTEMS 523 REV. 12-71																				

SK

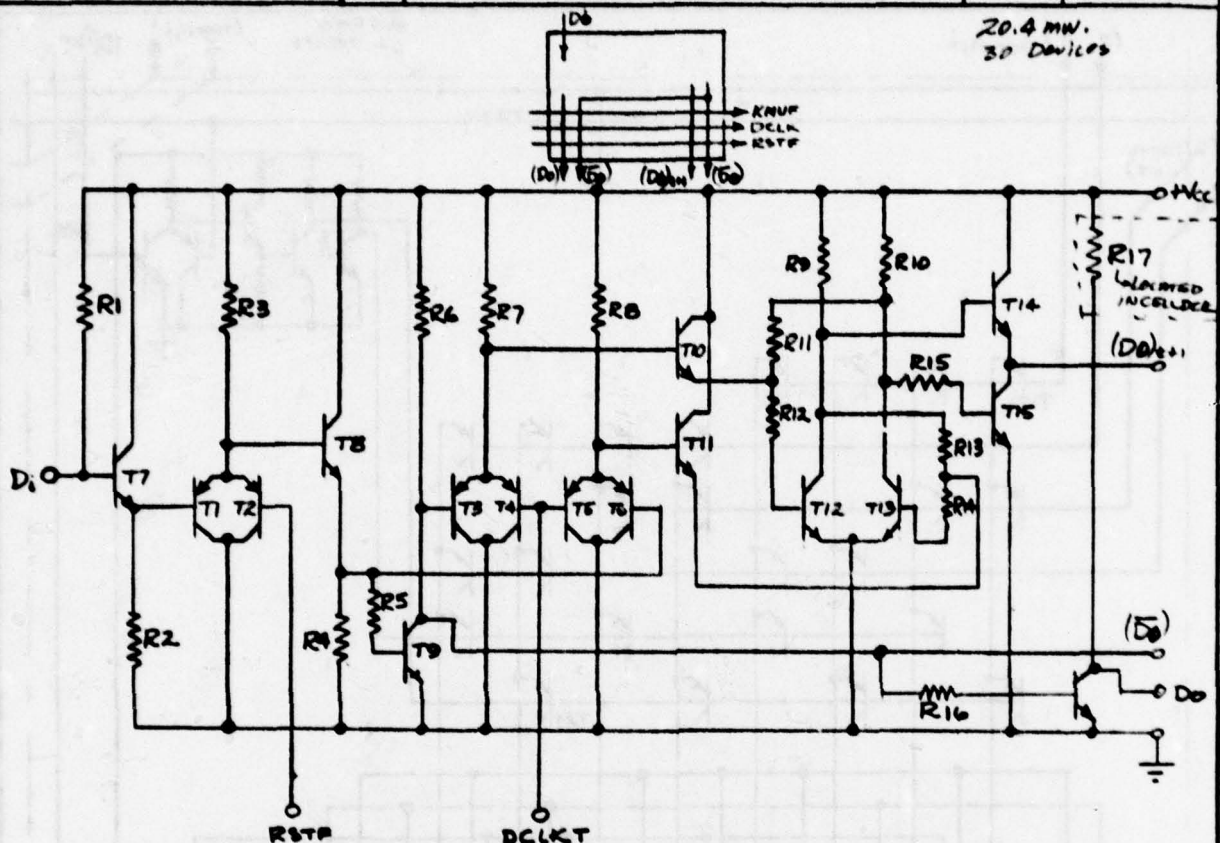
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

20.4 MW.
30 Devices

T1 - T6 = MODEL TP1
T7 - T15 = MODEL TN1

R1 = 50.

R2 = 5.

R3 = 10.

R4 = 4.

R5 = 3.

R6 = 4.

R7 = 10.

R8 = 10.

R9 = 5.

R10 = 2.5

R11 = 9.

R12 = 1.

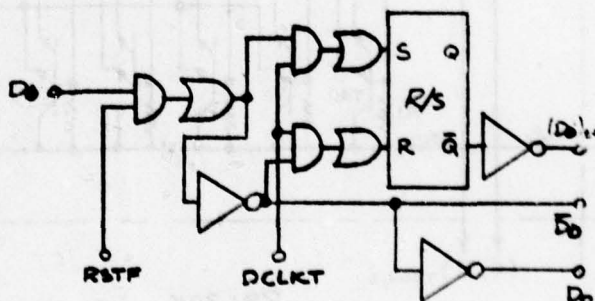
R13 = 9.

R14 = 1.

R15 = 10.

R16 = 40.

R17 = 15.



ENGINEERING SKETCH

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELL DE

SPA U

SIZE

CODE IDENT NO.

A

11982

SK

Figure 27

MJO

2349-71

SCALE

201

SHEET 1 OF

SYSTEMS 823 REV. 12/71

SK

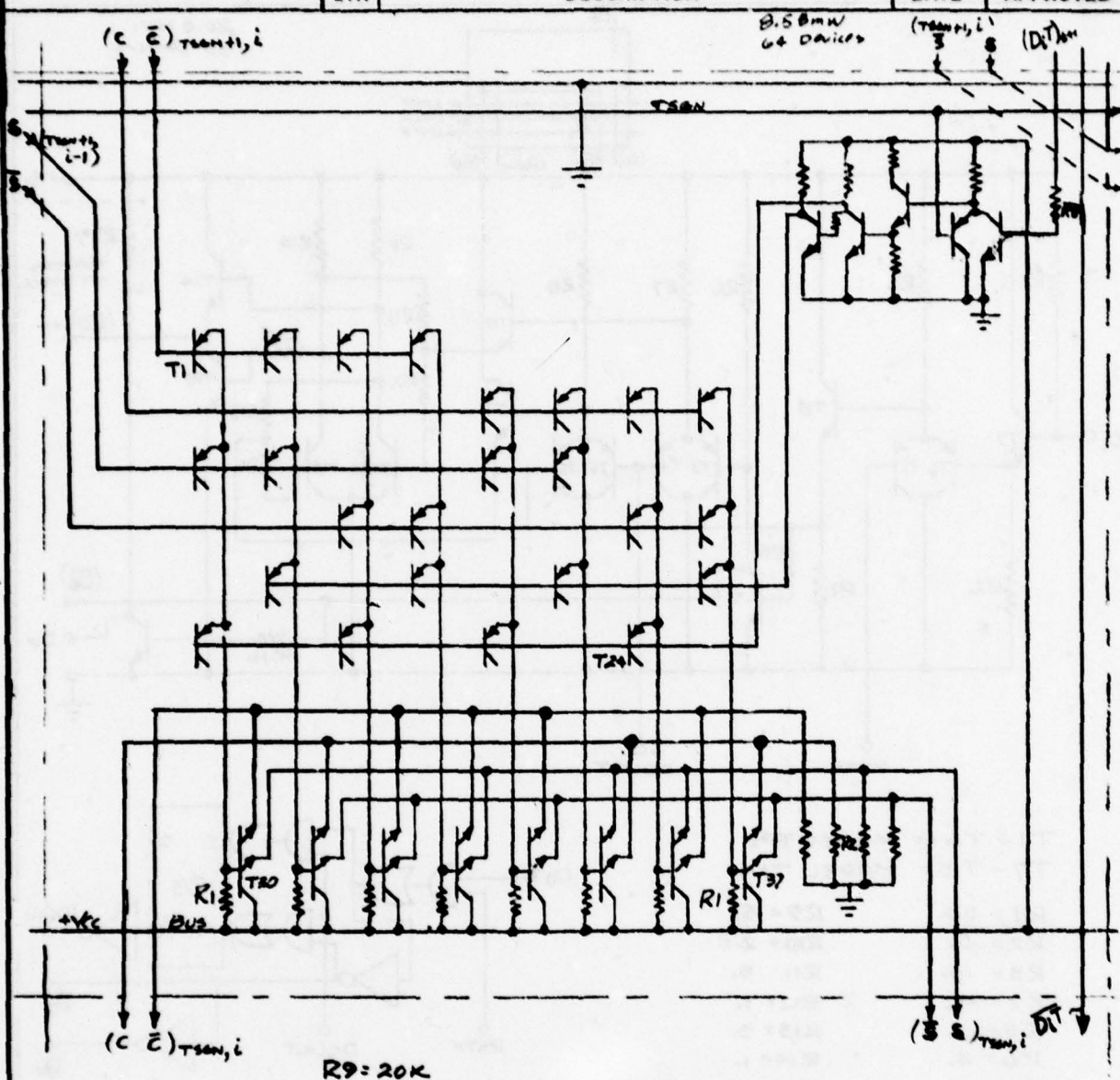
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

MJO

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLDX

SIZE

CODE IDENT NO.

A

11982

SK

Figure 28

SCALE

202

SHEET 1 OF

SYSTEMS 523 REV. 1 & 71

SK

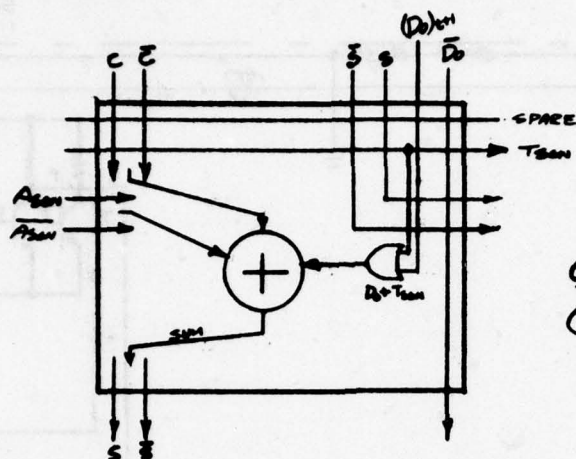
REVISIONS

LTR

DESCRIPTION

DATE

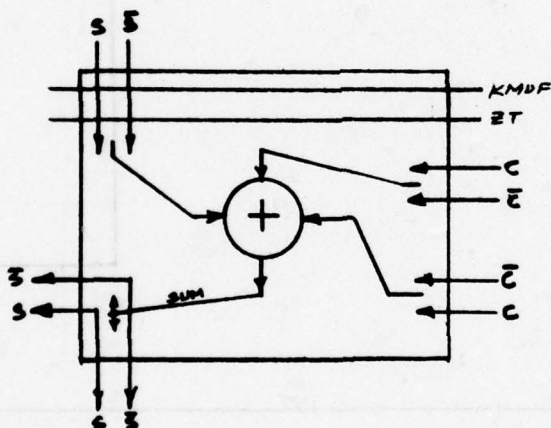
APPROVED



3.58 MW.
55 DEVICES

CELLEX

(SIMILAR TO CELLOX
BUT NO INPUT AND
NO CARRY OUTPUT



3.58 MW
52 DEVICES

CELLSXM

(SIMILAR TO
CELLSX)

ENGINEERING SKETCH

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLEX AND CELLSXM

SIZE

CODE IDENT NO.

A

11982

SK

Figure 29

MJO

SCALE

203

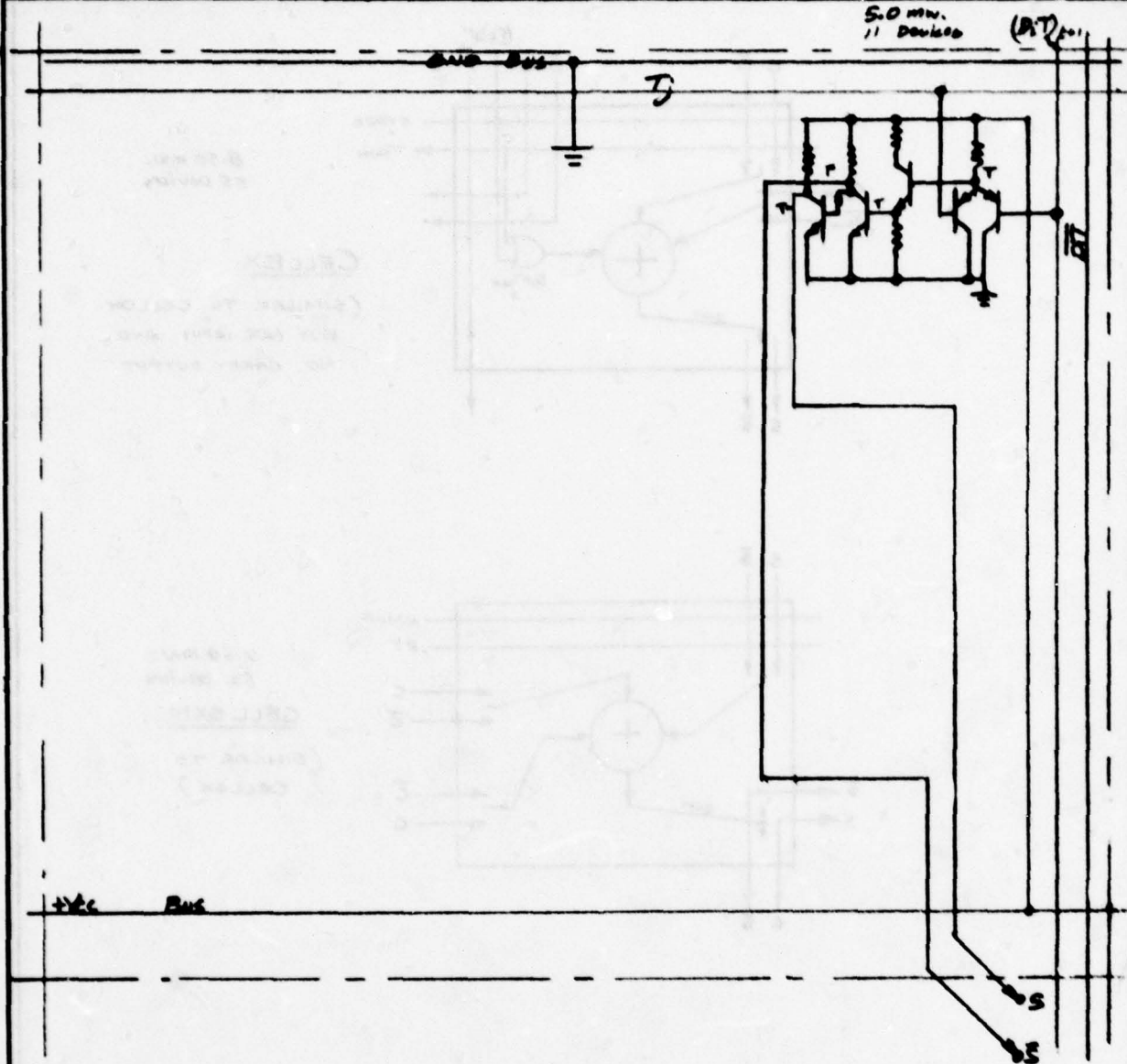
SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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5.0 mm.
11 Devices (B/T) 101



ENGINEERING SKETCH

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JMB

CELLFX

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 30

MJO

SCALE

204

SHEET 1 OF

SK

REVISIONS

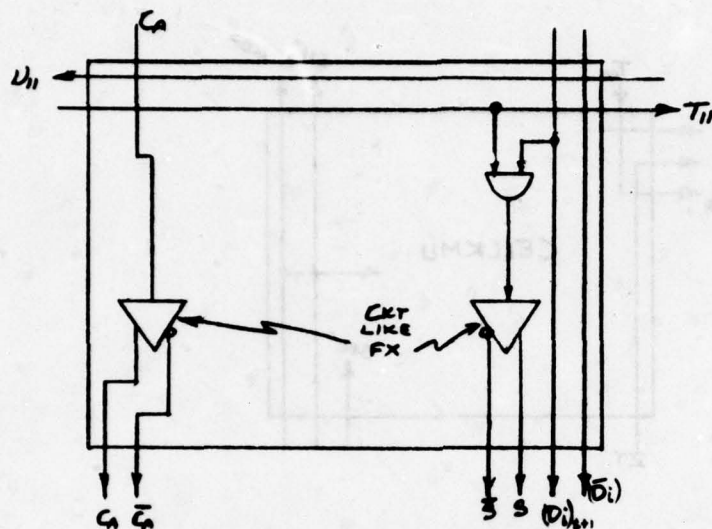
LTR

DESCRIPTION

DATE

APPROVED

10 mW.
20 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELL FXC
SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 31

SCALE

205

SHEET 1 OF

SK

REVISIONS

LTR

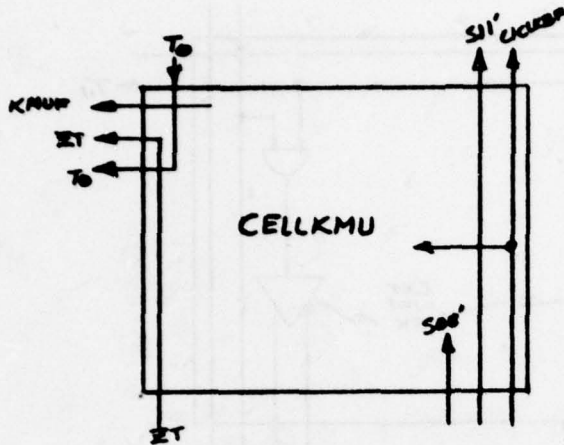
DESCRIPTION

DATE

APPROVED

$P_{DC(ave)} = 32 \text{ mw.}$

36 Devices



SIMILAR TO CELLCDB
BUT FOR BUSING

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JIB

CELLKMU

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 32

MJO

2349-71

SCALE

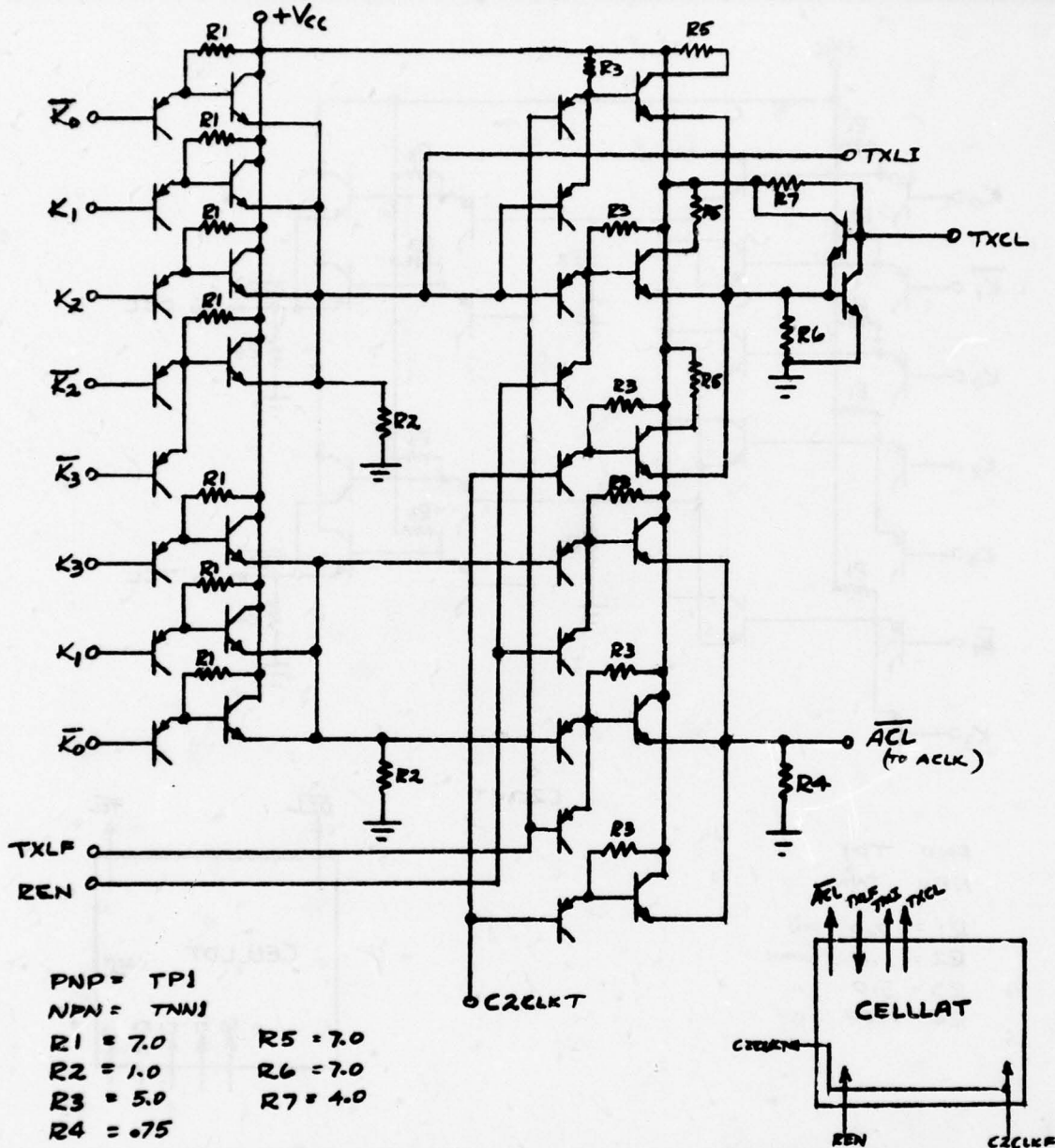
206

SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLAT

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 33

MJO

2349-71

SCALE

207

SHEET 1 OF

SK

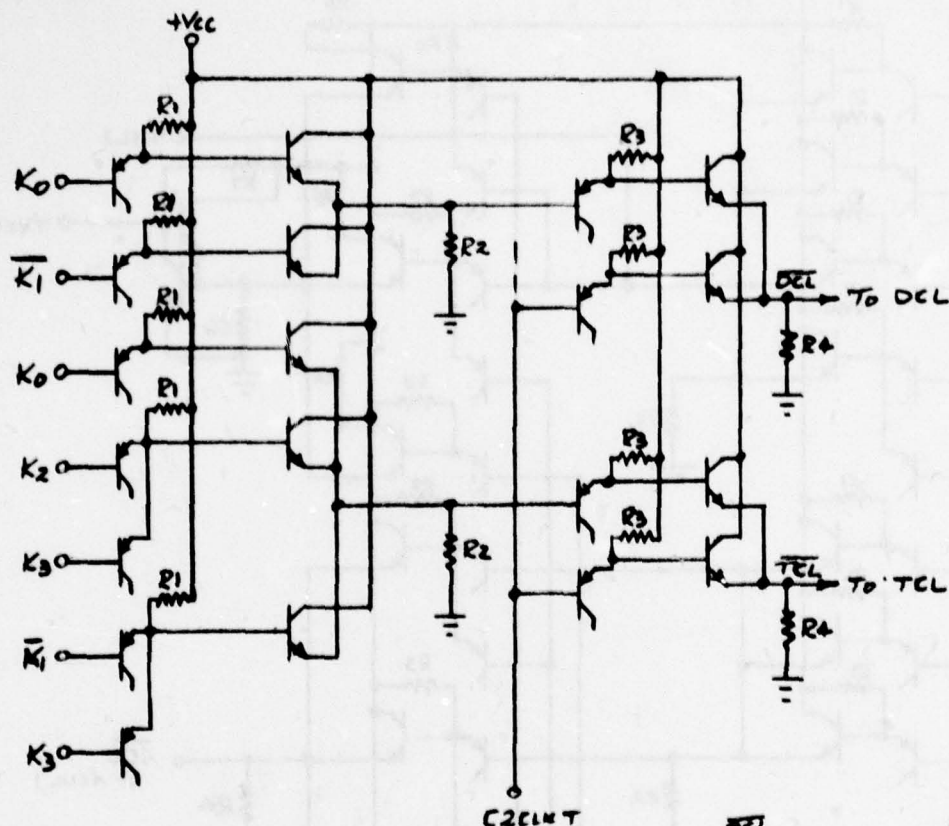
REVISIONS

LTR

DESCRIPTION

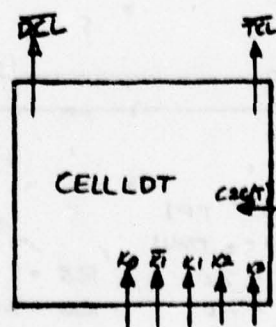
DATE

APPROVED



DNP TPJ
NPN TNNI

R1 = 7.0 PIN
R2 = 1.0 UNPIN
R3 = 5.0 "
R4 = .750 "



ENGINEERING SKETCH

ORIGINATOR

DATE

J.B.

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLDT

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 34

SCALE

208

SHEET 1 OF

SYSTEMS 523 REV. 12-71

SK

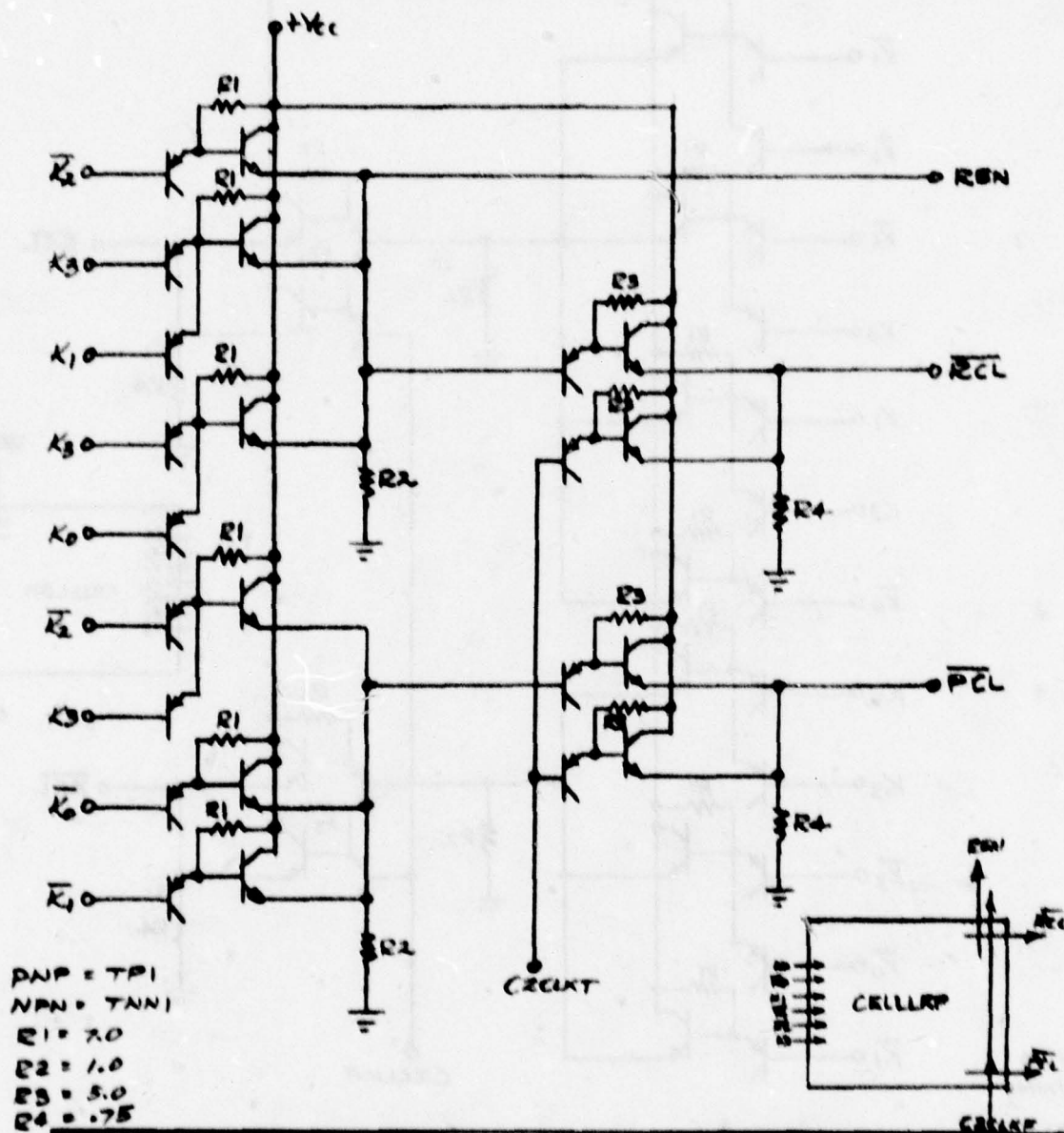
REVISIONS

LTR

DESCRIPTION

DATE _____

APPROVED



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE _____

CELLRP

S F M U

SIZE

CODE IDENT NO.

A

11982

SK

Figure 35

INFO

2949-71

SCALE

209

SHEET 1 OF

SYSTEMS AND NEW, 1971

SK

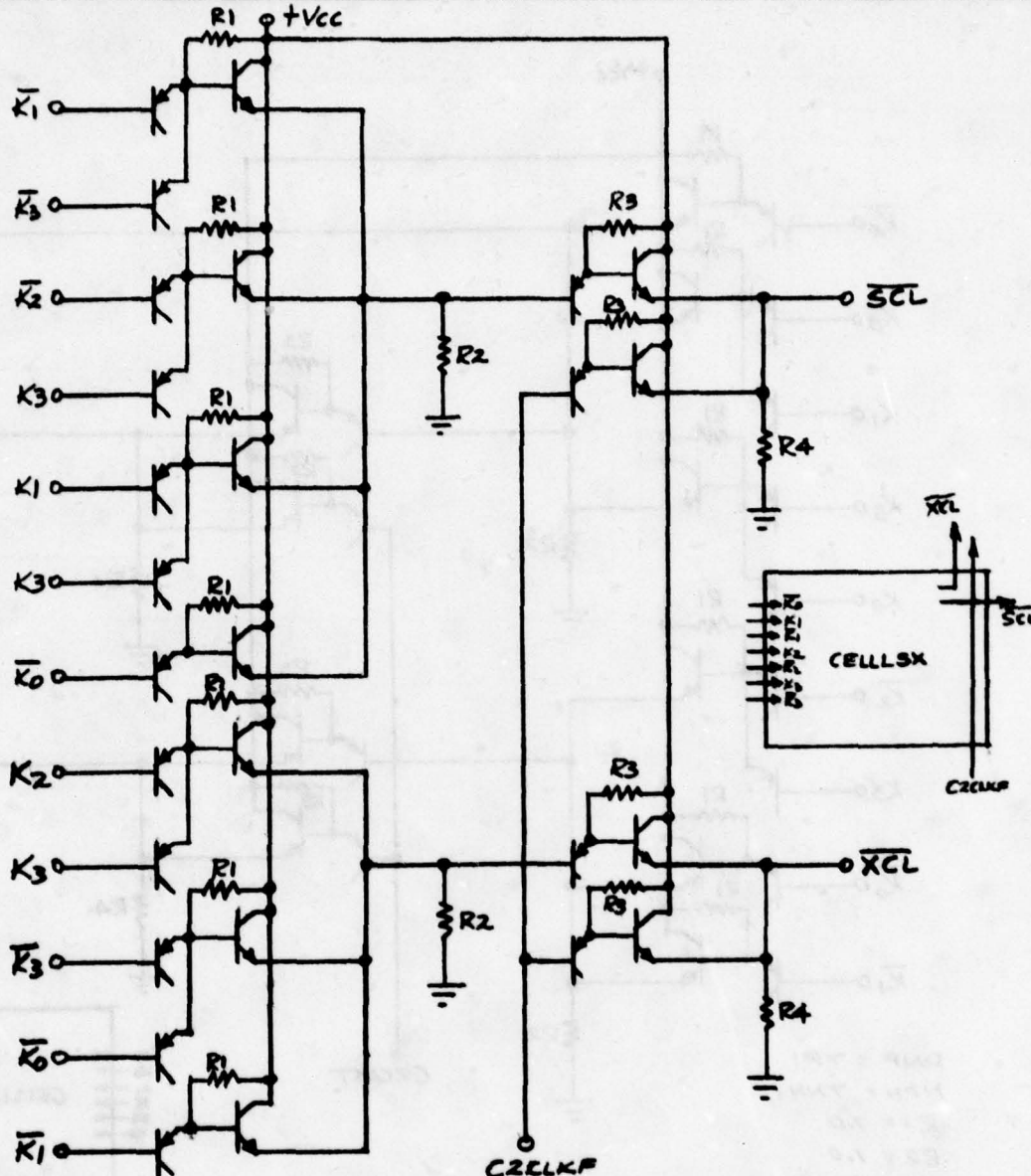
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



TP1
TNN1

R1 = 7.0
R2 = 1.0
R3 = 5.0
R4 = .75

ENGINEERING SKETCH

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDDING BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLSX

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 36

MJO

2349-71

SCALE

210

SHEET 1 OF

SYSTEMS 625 REV. 12-71

SK

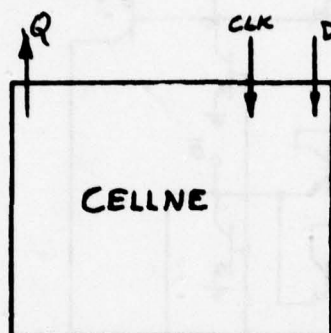
REVISIONS

LTR

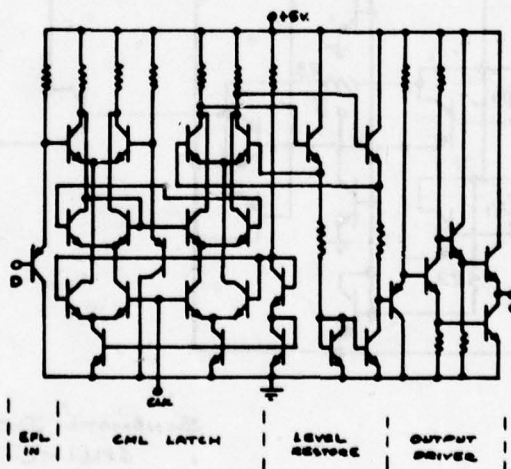
DESCRIPTION

DATE

APPROVED



SIMILAR TO CELL CDB



SINK > 5. mV.
SOURCE > 2.5 mV.
 $V_D = V_{SAT}$
 $V_I > 2.4$

*THIS IS A TEST
F/E CONNECTED
TO SEPARATE
TEST PAGE
LOCATION IS
ROW 2
COL 17*

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLNE

SPRU TEST F/E

SIZE

CODE IDENT NO.

A

11982

SK

Figure 37

MJO

2349-71

SCALE

211

SHEET 1 OF

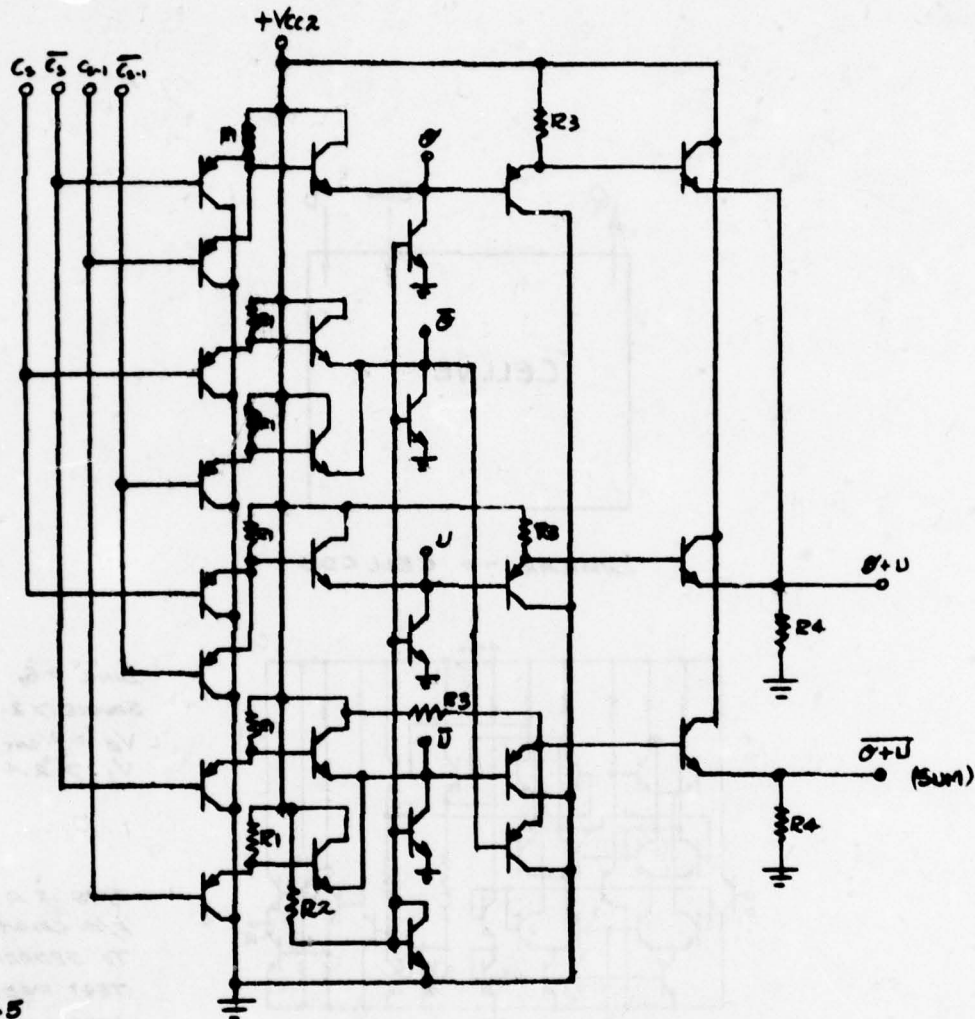
REVISIONS

LTR

DESCRIPTION

DATE _____

APPROVED



R1 = 17.5
R2 = 10.6
R3 = 5.6
R4 = 2.5

SCHEMATIC INCORPORATED IN
CELLME

ENGINEERING SKETCH

ORIGINATOR

DATE _____

ΔIB

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

LIMITER CONTROL LOGIC
(OVERFLOW, UNDERFLOW, SUM) SEE
SPAUC CELL LMC

SIZE	CODE	IDENT	NO.
------	------	-------	-----

A | 11982

SK

Figure 38

MLJO

2349-71

SCALE 212

SHEET 1 OF

SK

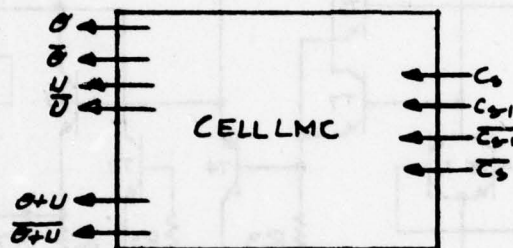
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



FOR CIRCUIT SEE
LIMITER CONTROL
LOGIC

ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELL MC	
JIB		GPAU	
		SIZE	CODE IDENT NO.
		A	11982
MJO		SCALE	213
2349-71			SK Figure 39
		SHEET 1 OF	

SK

REVISIONS

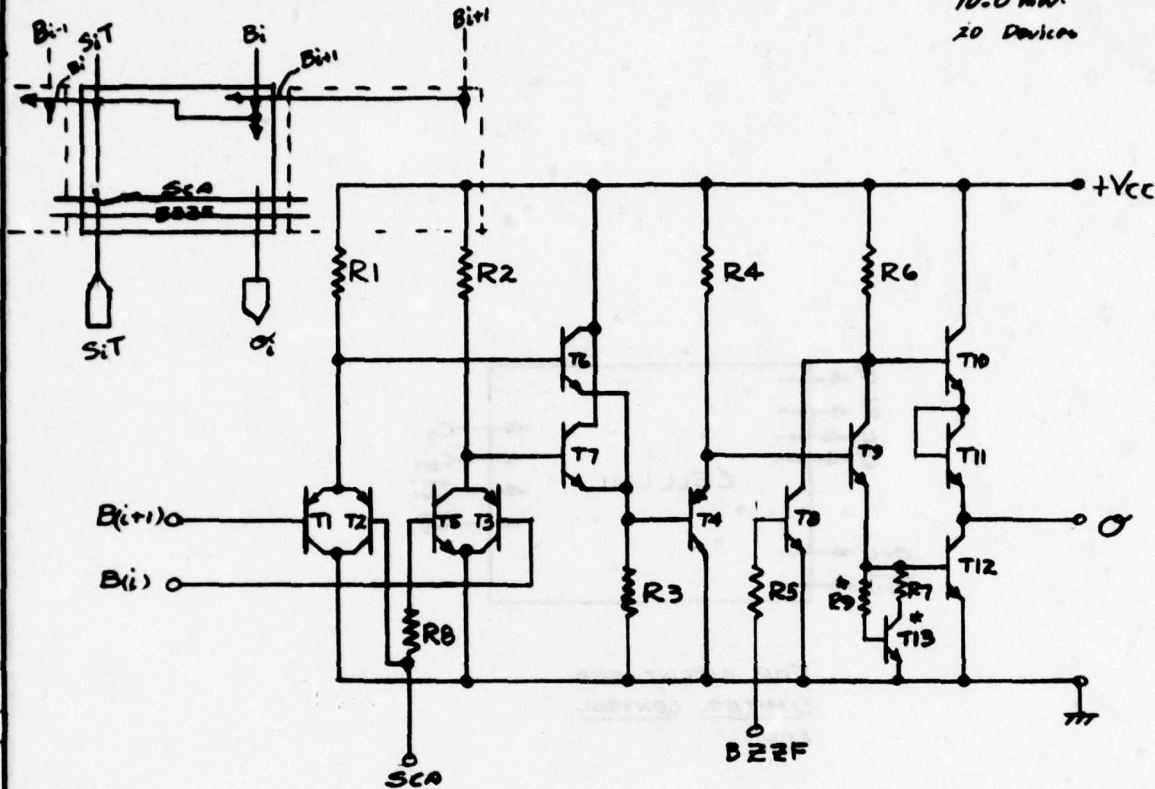
LTR

DESCRIPTION

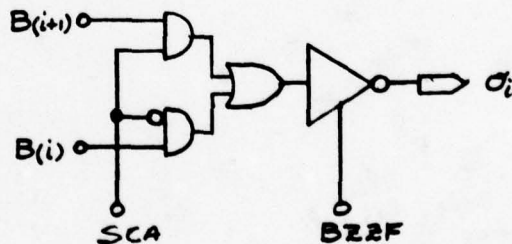
DATE

APPROVED

10.0 mW.
20 Devices



T1 - T4 = MODEL TP1
 T5 - T11 = MODEL TNN1
 T12 = 3 TNN1 IN PARALLEL
 R1 = 10.
 R2 = 10.
 R3 = 4.
 R4 = 16.0
 R5 = 5.0
 R6 = 3.0
 R7 = 2.4
 R8 = 20.
 R9 = 1.6



ENGINEERING SKETCH

ORIGINATOR

DATE

JLB

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLO

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 40

SCALE

214

SHEET 1 OF

SK

REVISIONS

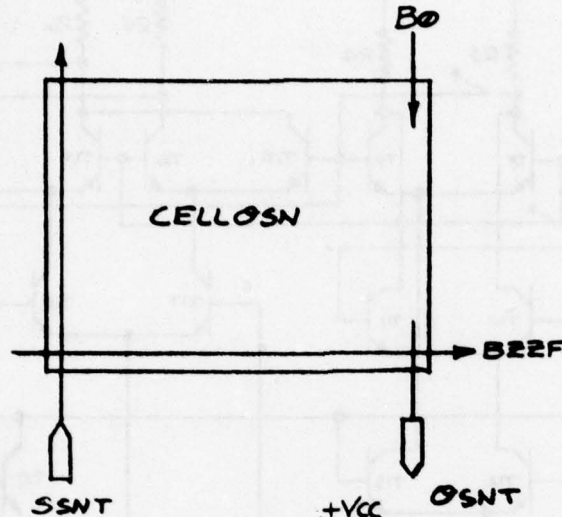
LTR

DESCRIPTION

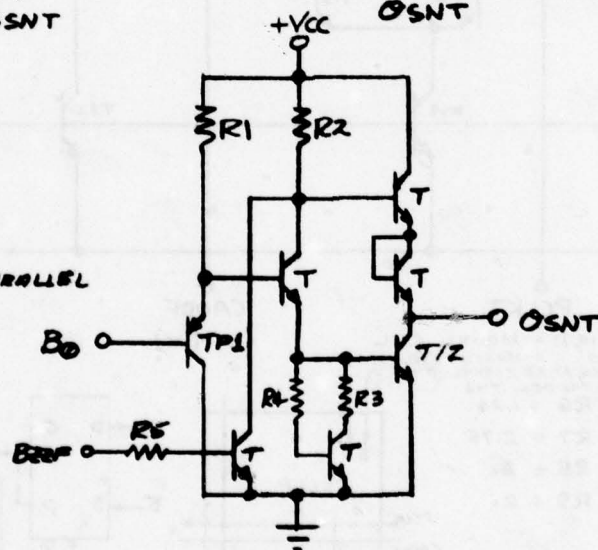
DATE

APPROVED

3.9 mw.
8 Devices



T = TANI
T12 = 3 TANI IN PARALLEL
R1 = 10.
R2 = 3.0
R3 = 2.4
R4 = 1.6
R5 = 5.0



ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

MJO

2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLOS

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 41

SCALE

215

SHEET 1 OF

SK

REVISIONS

LTR

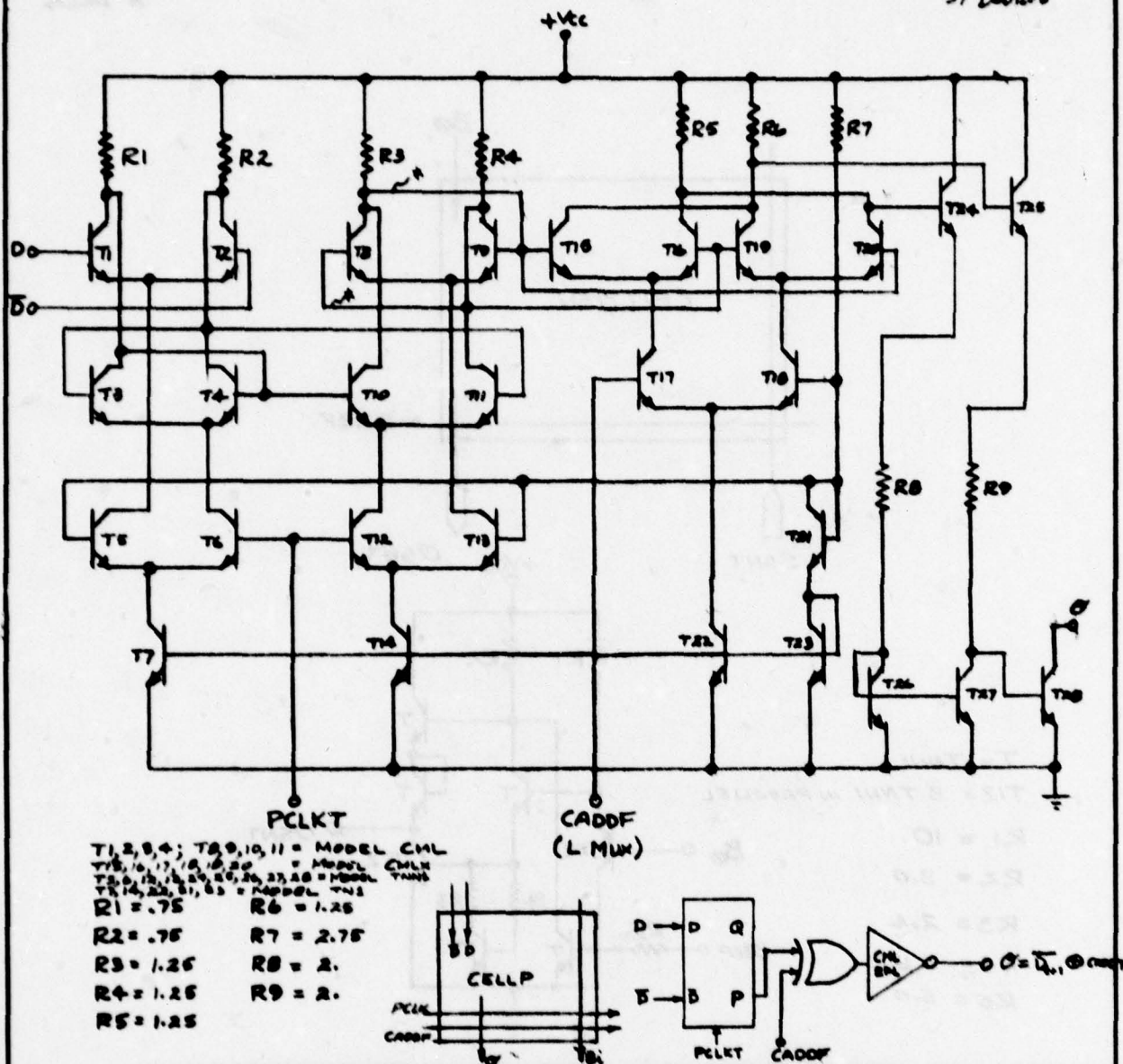
DESCRIPTION

DATE

APPROVED

34. & MW.

37 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

J.B.

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CML DTYPE F/F
 WITH EX. OR GATE & RESTORE
 CELLP SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 42

SCALE

216

SHEET 1 OF

SYSTEMS GROUP, 10/74

SK

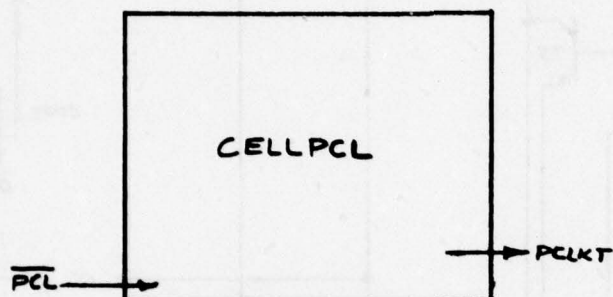
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

37.7 mw.
25 DevicesSAME AS CELLXCL
EXCEPT FOR BUSING

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JLB

CELLPCL

SPAUI

SIZE

CODE IDENT NO.

A

11982

SK

Figure 43

MJO

2349-71

SCALE

217

SHEET 1 OF

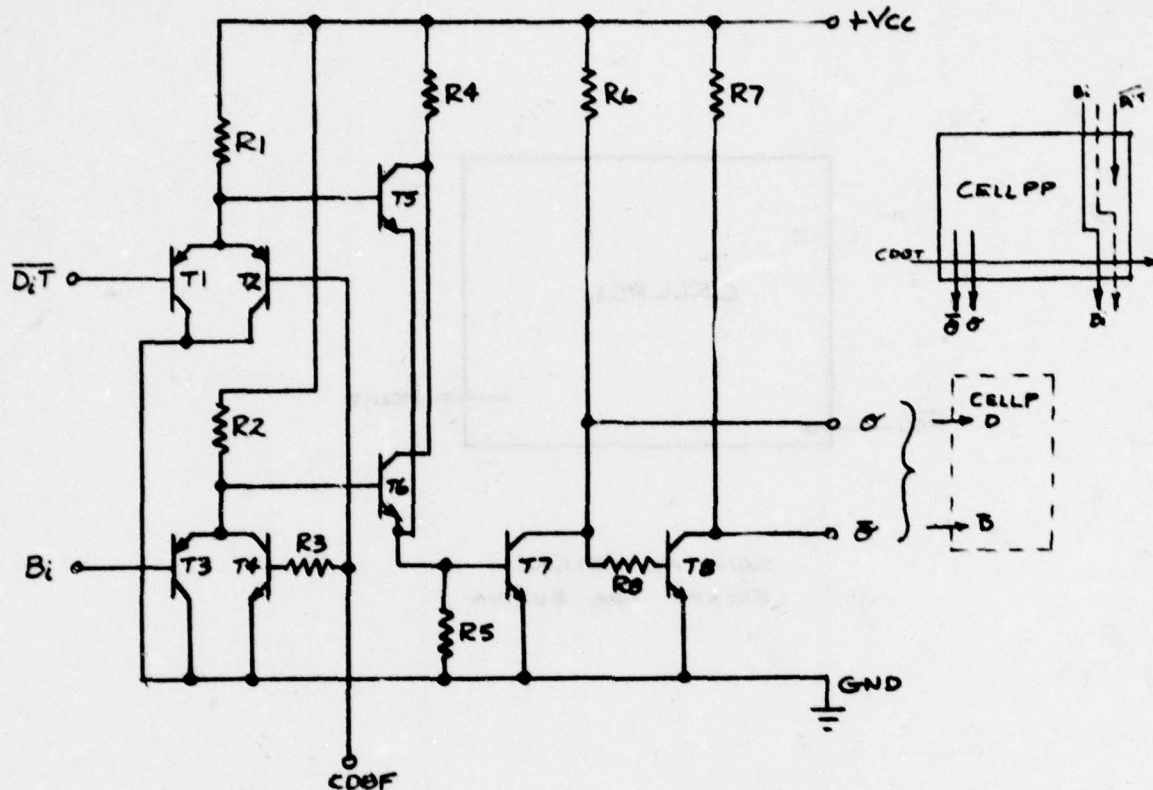
SYSTEMS 103 REV. 12-71

SK

REVISIONS

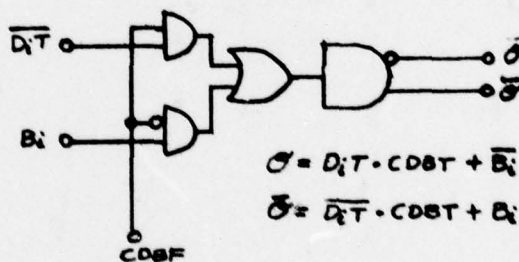
LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------

15.8 mw.
16 Devices.



T1 - T3 = MODEL TP1
T4 - T8 = MODEL TNN1

R1 = 10. R6 = 10.
R2 = 10. R7 = 16.
R3 = 20. R8 = 20.
R4 = 10.
R5 = 4.



$$O = D_iT \cdot CDBT + \overline{B_i} \cdot \overline{CDBT}$$

$$B = \overline{D_iT} \cdot CDBT + B_i \cdot \overline{CDBT}$$

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLPP

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 44

MJO

2349-71

SCALE

218

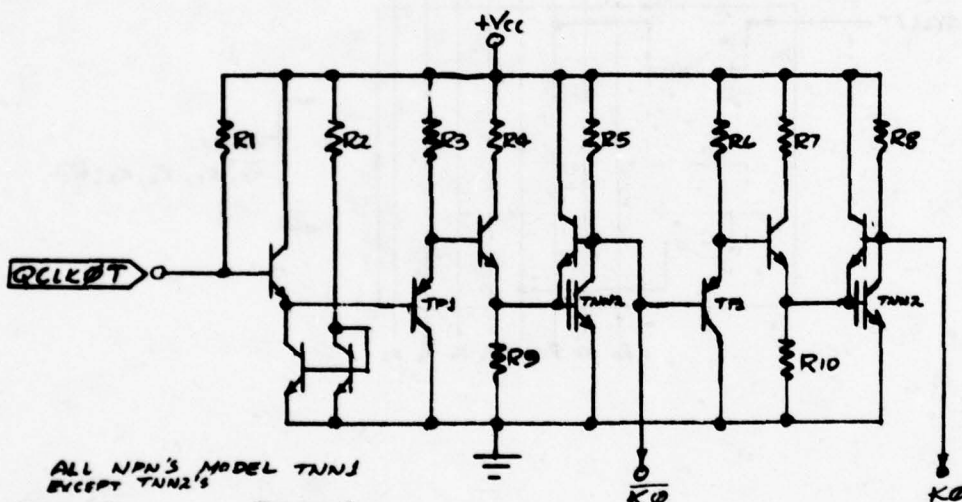
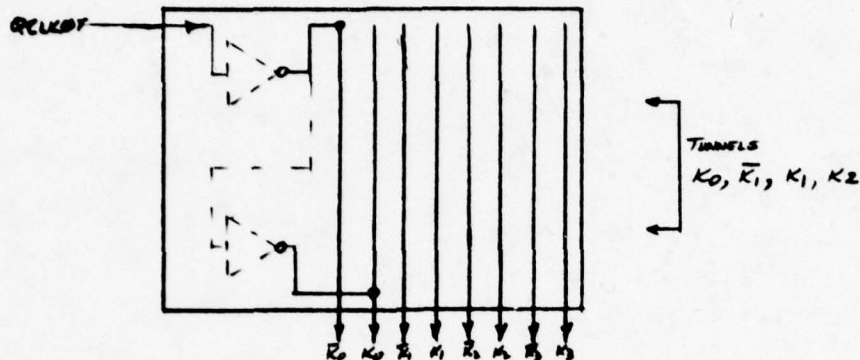
SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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$P_D = 58.7 \text{ mW}$
42 Devices



ALL NPN'S MODEL TUNJ
EXCEPT TUN2'S

R1 = 50.0 R8 = 1.8
R2 = 18.0 R9 = 4.0
R3 = 5.0 R10 = 4.0
R4 = 3.0
R5 = 1.8
R6 = 5.0
R7 = 3.0

I SINK 2.4 mV.
I SOURCE 2.5 mV.

ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELL QC0	
J.B.		SPAU	
SIZE	CODE IDENT NO.	SK Figure 45	
A	11982		
SCALE	219	SHEET 1 OF	
2349-71			

SK

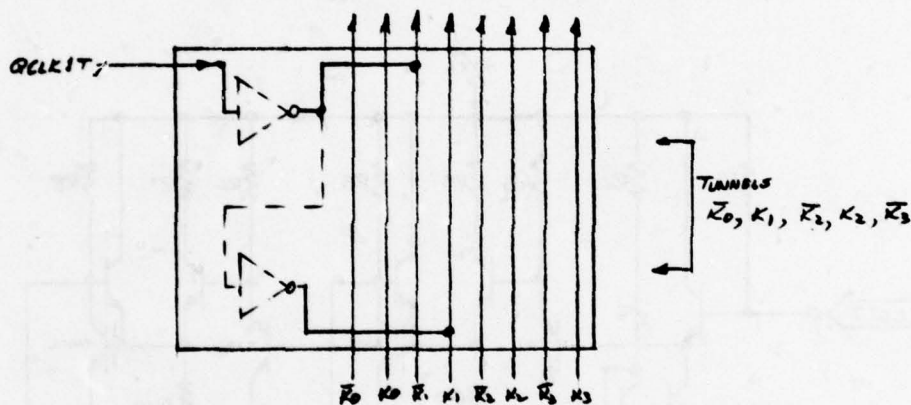
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JIB

CELL QC1

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 46

MJO

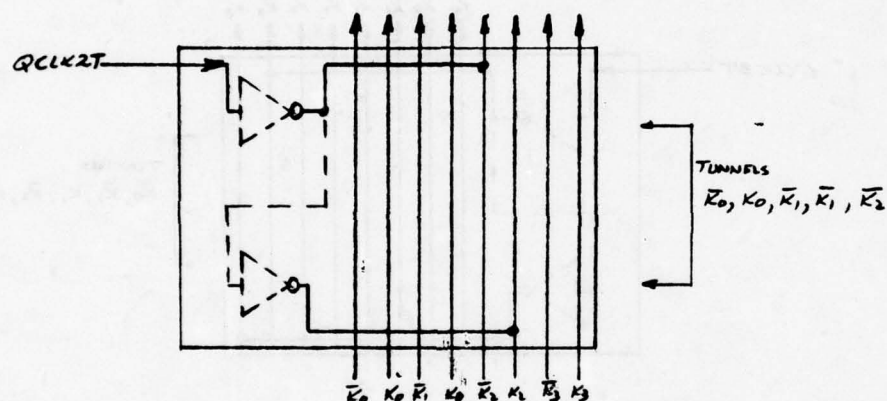
2349-71

SCALE

220

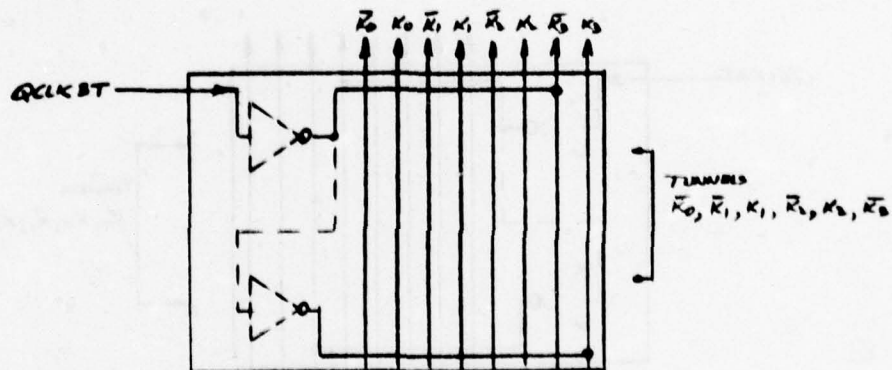
SHEET 1 OF

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELL QCL2	
JIB		SPAU	
		SIZE A	CODE IDENT NO. 11982
		SK	Figure 47
MJO	2349-71	SCALE 221	SHEET 1 OF

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



CELLQCB

LIKE QCB EXCEPT
FOR CONNECTION

ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLQCB	
<i>JMB</i>		SPAU	
		SIZE	CODE IDENT NO.
		A	11982
MJO	2349-71	SK	Figure 48
		SCALE	SHEET 1 OF
		222	

SK

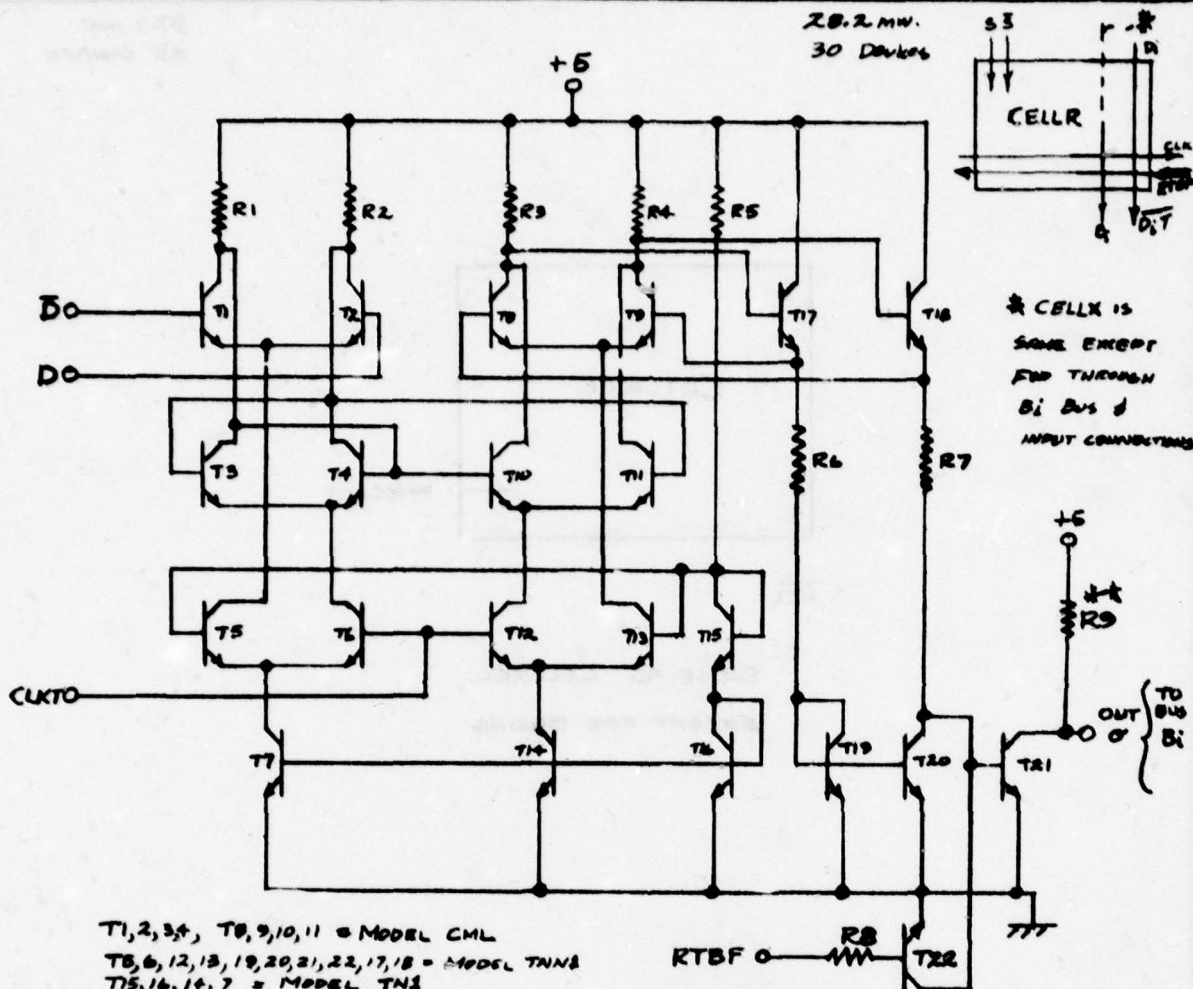
REVISIONS

LTR

DESCRIPTION

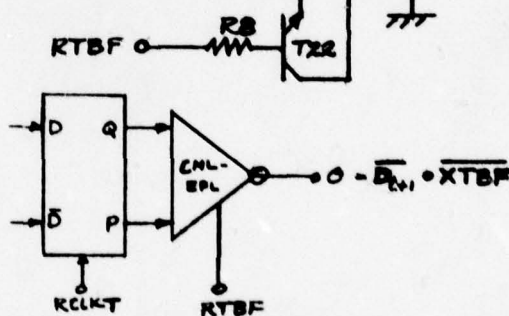
DATE

APPROVED



T1,2,3,4, T8,9,10,11 = MODEL CML
T5,6,12,13,19,20,21,22,17,18 = MODEL TNNA
T15,16,14,7 = MODEL TN1

R1 = .75 R9 = 5.0 *
R2 = .75
R3 = 1.25 * * CELLR ONLY
R4 = 1.25 HAS BUS TERMINATING
R5 = 2.75 RESISTOR, R9
R6 = 2.
R7 = 2.
R8 = 5.



ENGINEERING SKETCH

ORIGINATOR

DATE

MB

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CML D TYPE FF

CELLR

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 49

MJO

2549-71

SCALE

223

SHEET 1 OF

SK

REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

37.7 mw
25 Devices

CELLRCL

RCL

RCLKT

SAME AS CELLXCL
EXCEPT FOR BUSING

ENGINEERING SKETCH

ORIGINATOR

DATE

JB

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLRCL

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 50

MJO

2349-71

SCALE

224

SHEET 1 OF

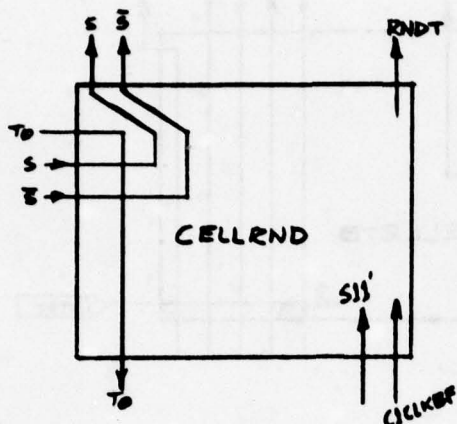
SYSTEMS DES REV. 10-71

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------

32 mm.
36 Devices



SIMILAR TO CELLCDB
BUT FOR PHASE REVERSAL
ON OUTPUT AND BUSING

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

MB

CELLRND

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 51

MJO

2349-71

SCALE

225

SHEET 1 OF

SK

REVISIONS

LTR

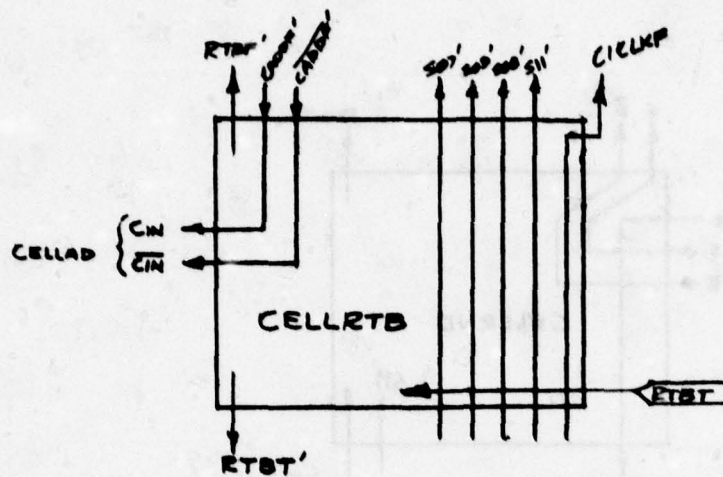
DESCRIPTION

DATE

APPROVED

42.7 MW

44 Drivers



RTBT' & RTBT ARE CASCADED
 CIRCUITS SAME AS CELLAD
 EXCEPT OUTPUT CLAMPED TO
 "0" = V_{SAT} ; "1" = $2V_{DD}$

ENGINEERING SKETCH

TRW
 SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLRTB

SPMU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 52

MJO

2349-71

SCALE

226

SHEET 1 OF

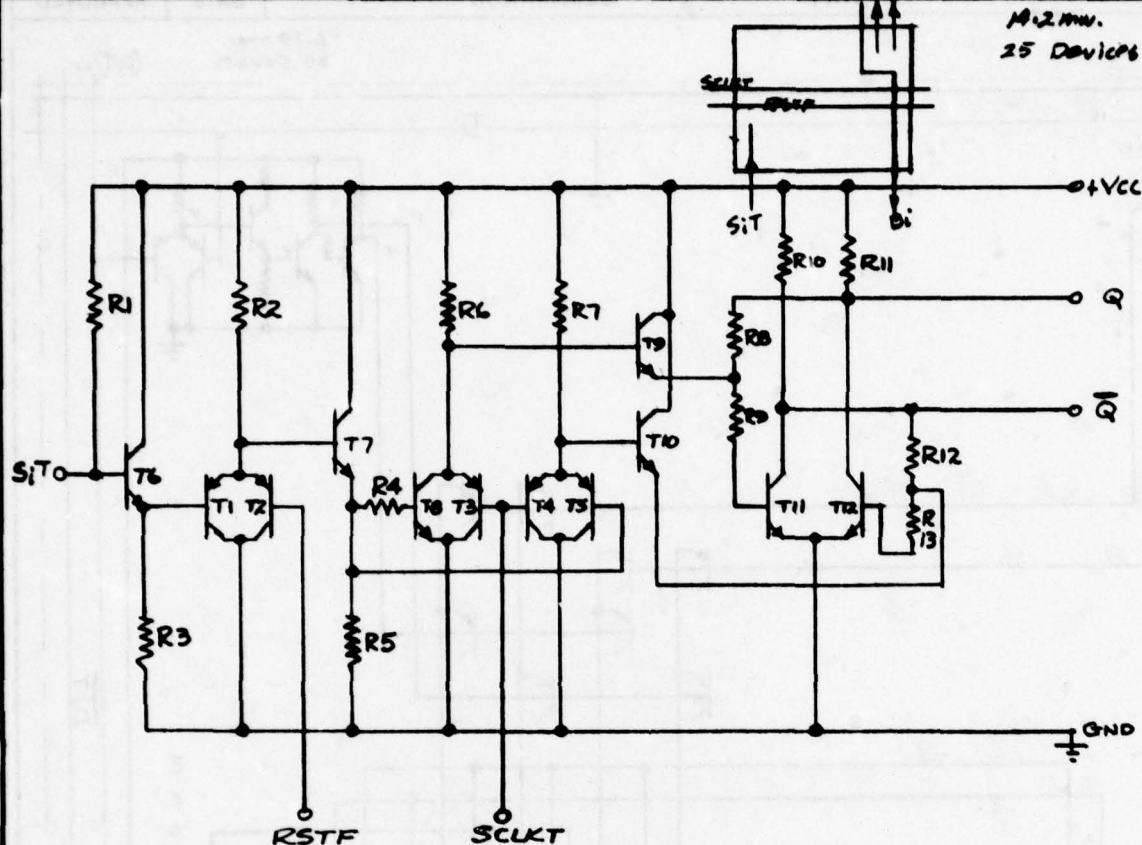
SYSTEMS GROUP REV. 12/71

SK		REVISIONS		
LTR	DESCRIPTION	DATE	APPROVED	
<div style="text-align: right; margin-bottom: 10px;"> <i>6.79 MW. 35 Devices</i> (D.T.) </div>				
ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR <i>JUB</i>	DATE	CELLRX SPAU		
MJO	DATE	SIZE A	CODE IDENT NO. 11982	SK Figure 53
SCALE		227	SHEET 1 OF	

SK

REVISIONS

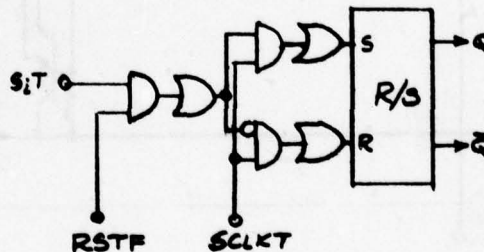
LTR	DESCRIPTION	Q Q	DATE	APPROVED
-----	-------------	-----	------	----------



10.2 MW.
25 Devices

T1 - T5 = MODEL TP1
T6 - T12 = MODEL TN1

R1 = 50. R8 = 19.
R2 = 10. R9 = 1.
R3 = 5. R10 = 10.
R4 = 10. R11 = 10.
R5 = 4. R12 = 19.
R6 = 10. R13 = 1.
R7 = 10.



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLS

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 54

MJO

2349-71

SCALE

228

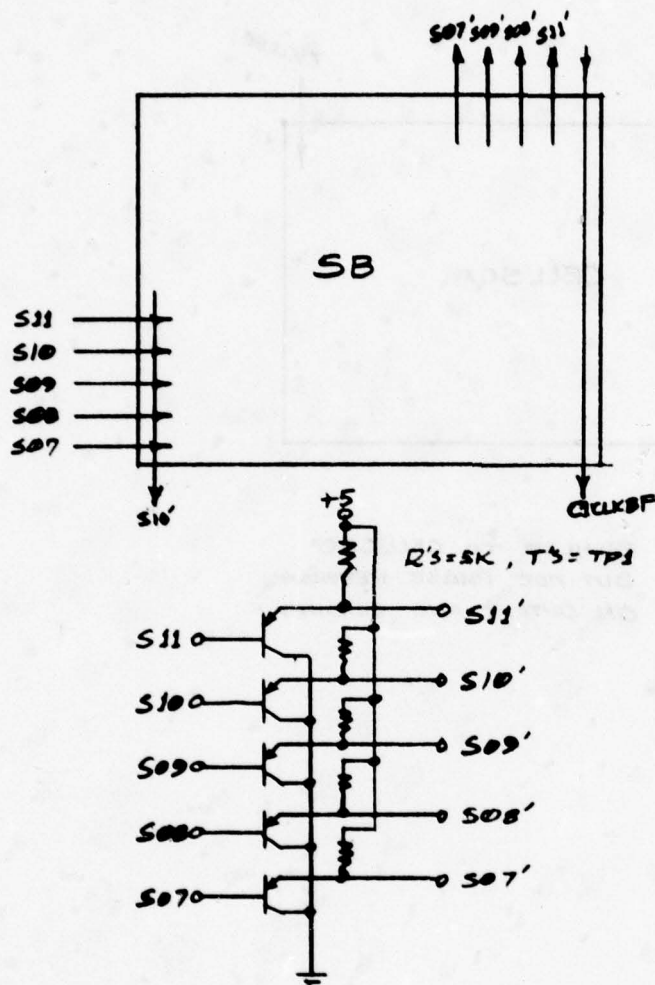
SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------

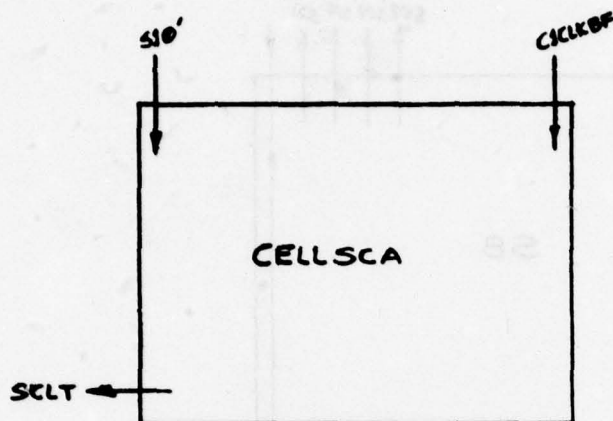
12.5 mm
10 devices



ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLSB	
JLB		SPAU	
		SIZE	CODE IDENT NO.
		A	11982
		SK	Figure 55
MJO		SCALE	SHEET 1 OF
		229	

SK	REVISIONS		
	LTR	DESCRIPTION	DATE APPROVED

32 MW.
36 Devices



SIMILAR TO CELLCDB
BUT FOR PHASE REVERSAL
ON OUTPUT AND BUSING

ENGINEERING SKETCH		TRW <small>SYSTEMS GROUP</small> ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLSCA	
JMB		SPAU	
		SIZE	CODE IDENT NO.
		A	11982
MJO	2349-71	SK	Figure 56
		SCALE	SHEET 1 OF
		230	

SK

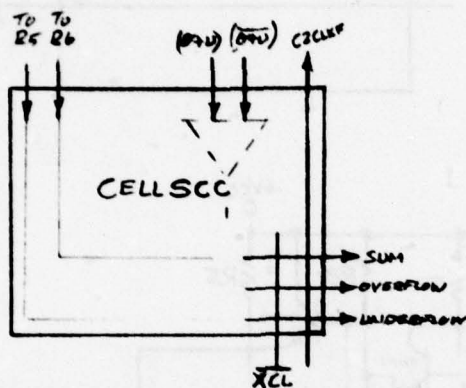
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



FOR CIRCUIT SEE OVERFLOW
CONTROL CIRCUIT

OUTPUT: $SUM = (D+U)$

ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELL SCC

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 57

MJO

2349/71

SCALE

231

SHEET 1 OF

SYSTEMS 823 REV. 12-71

SK

REVISIONS

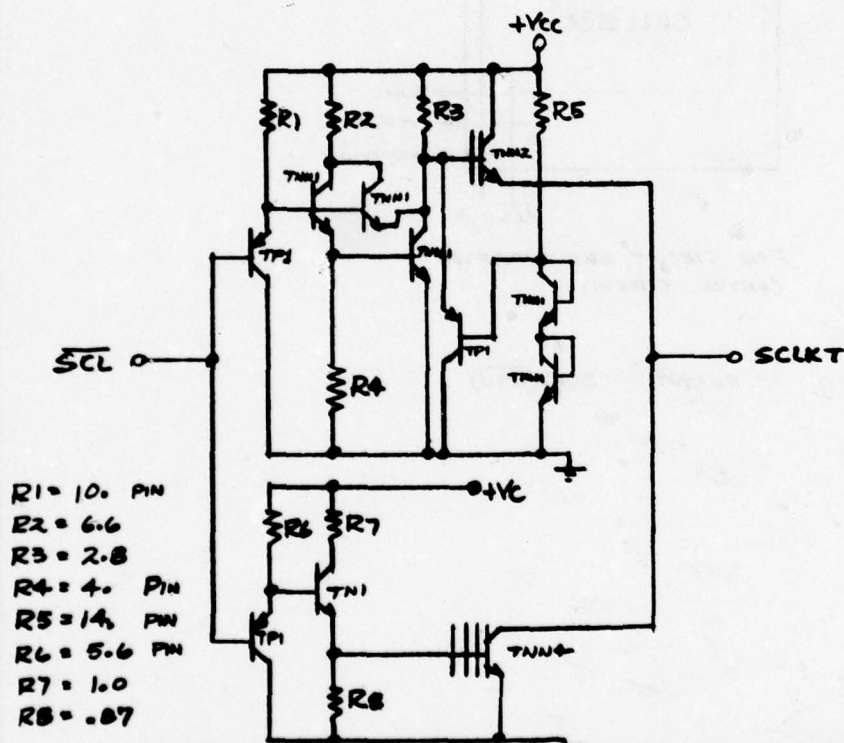
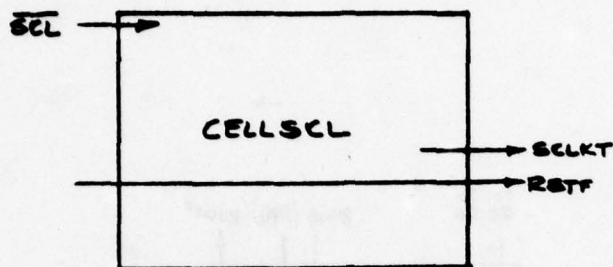
LTR

DESCRIPTION

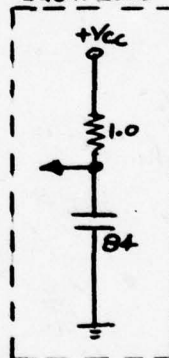
DATE

APPROVED

29.7 mW
22 Devices



EQUIV. LOAD



7 mΩ. SOURCE
16 mΩ. SINK
 $V_D = V_{SAT}$
 $V_i = 2V_{BE}$

ENGINEERING SKETCH

ORIGINATOR

DATE

JAB

MJO

2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLSCL

SPV

SIZE

A

CODE IDENT NO.

11982

SK

Figure 58

SCALE

232

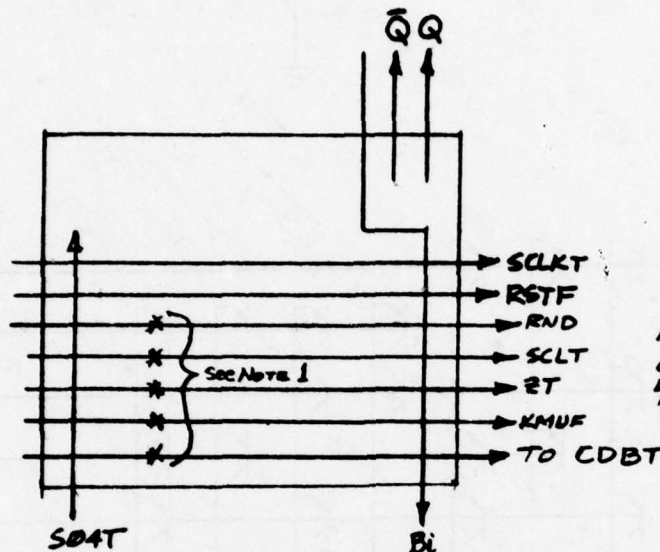
SHEET 1 OF

SYSTEMS 803 REV. 12-71

SK

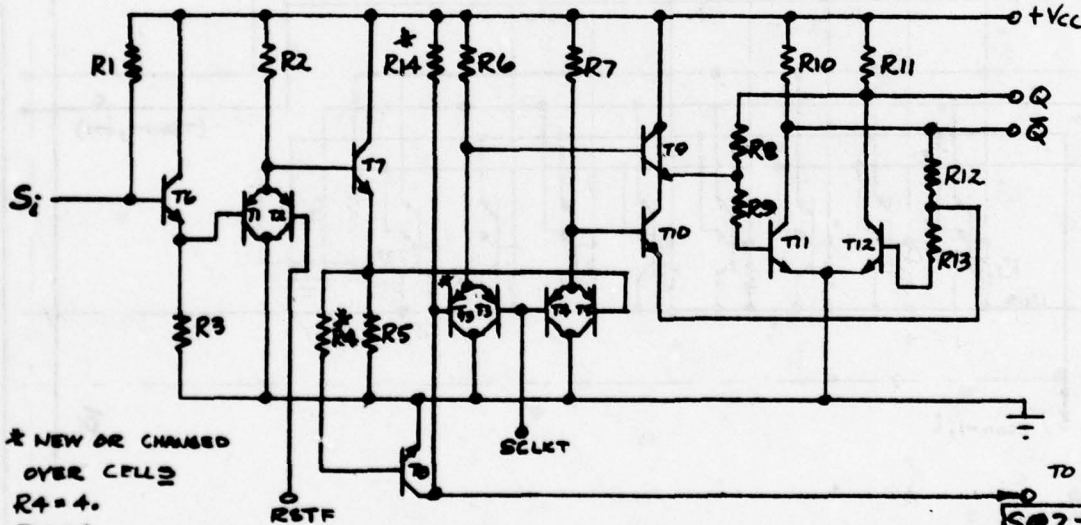
REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
		14.2 MW.	
		25 Devices	



Notes:
 CONTACTS ARE
 DEFINED IN
 PADCELL -
 CONTACTS VS. BIT SIGNIF.

RND @ 11
 SCLT @ 10
 ET @ 9
 KMUF @ 8
 CDBT @ 7



* NEW OR CHANGED
 OVER CELL 3
 R4 = 4.
 R14 = 4.
 T13 = TP1

TO CONFIGURATION
 REG.
 S02 -> CDBT

ENGINEERING SKETCH

TRW
 SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR DATE

JB

CELL SNC

SPAU

SIZE CODE IDENT NO.
A 11982

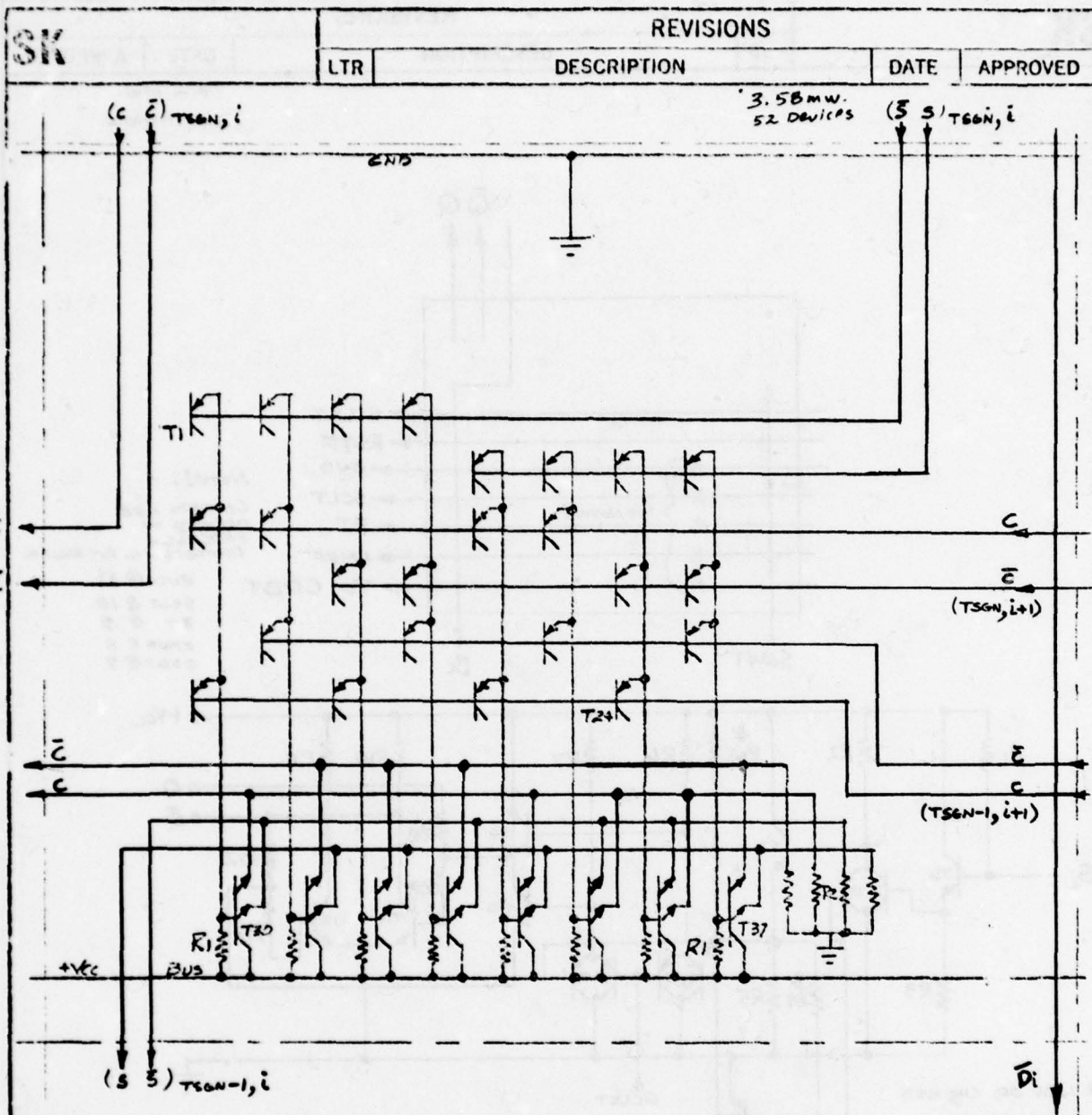
SK

Figure 59

MJO 2349-71

SCALE 233

SHEET 1 OF



ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CELLSX	
JLB		SPAU	
		SIZE	CODE IDENT NO.
		A	11982
MJO		SK	Figure 60
SCALE		234	SHEET 1 OF

SK

REVISIONS

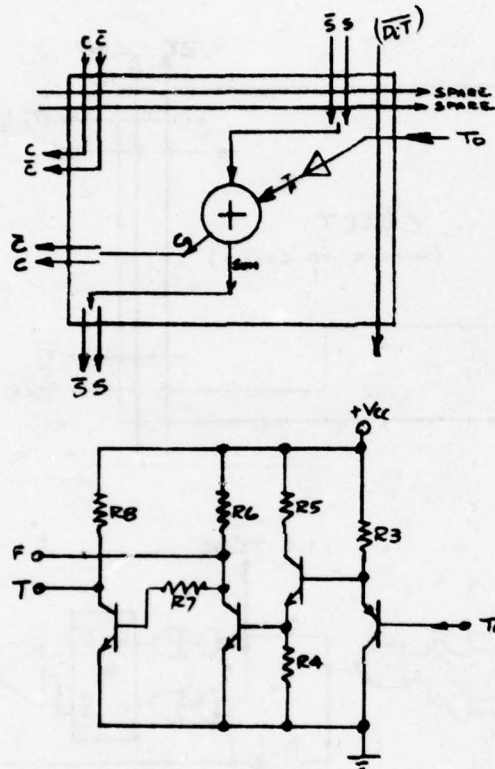
LTR

DESCRIPTION

DATE

APPROVED

0.50 mw.
62 Devices



ALL T's TPJ OR TNS

- R3 = 20.
- R4 = 4.
- R5 = 10.
- R6 = 10.
- R7 = 40.
- RB = 15.

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLSXL

MJO

SIZE

CODE IDENT NO.

A

11982

SK

Figure 61

SCALE

235

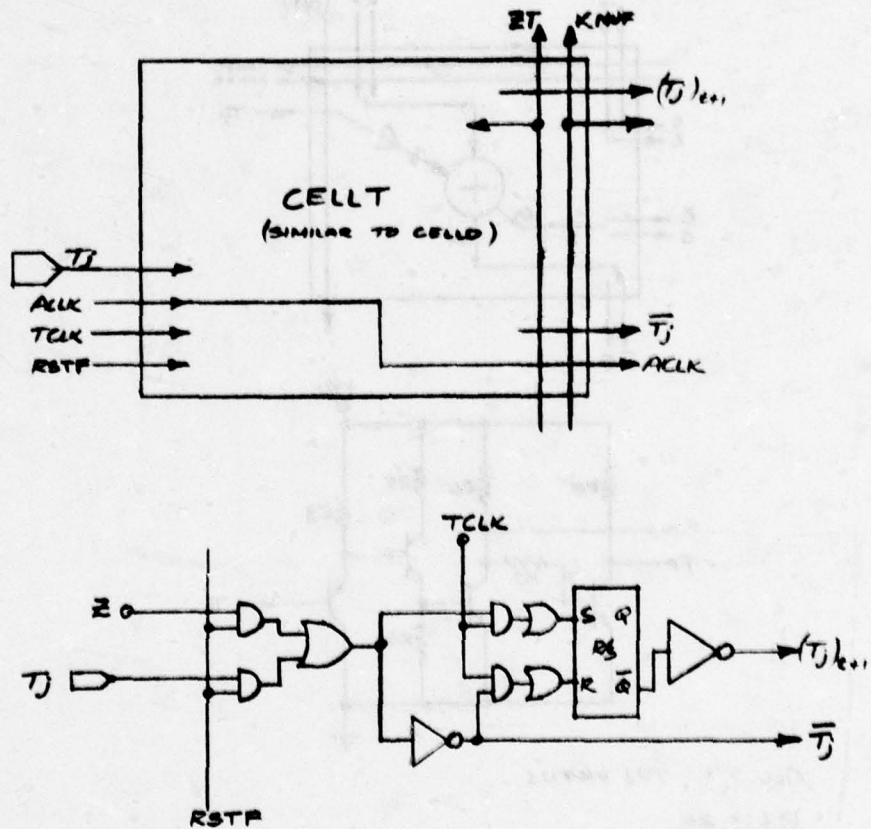
SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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20.4 MW.
30 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

J.B.

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELL T

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 62

SCALE

236

SHEET 1 OF

SYSTEMS GROUP REV. 12/71

SK

REVISIONS

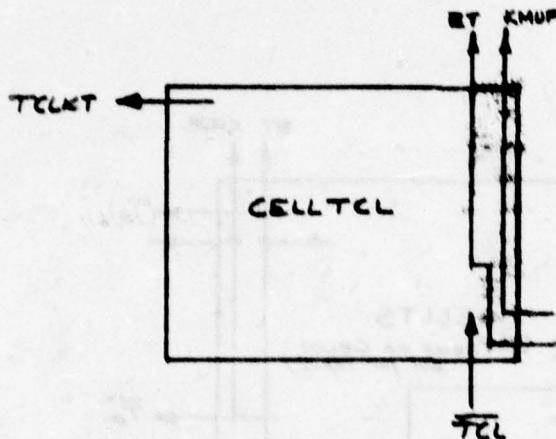
LTR

DESCRIPTION

DATE

APPROVED

29.7 mw.
22 Devices



SAME AS CELLOCL
EXCEPT FOR BUSHING

ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLTEL

SRMU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 63

MJO

2349-71

SCALE

237

SHEET 1 OF

SK

REVISIONS

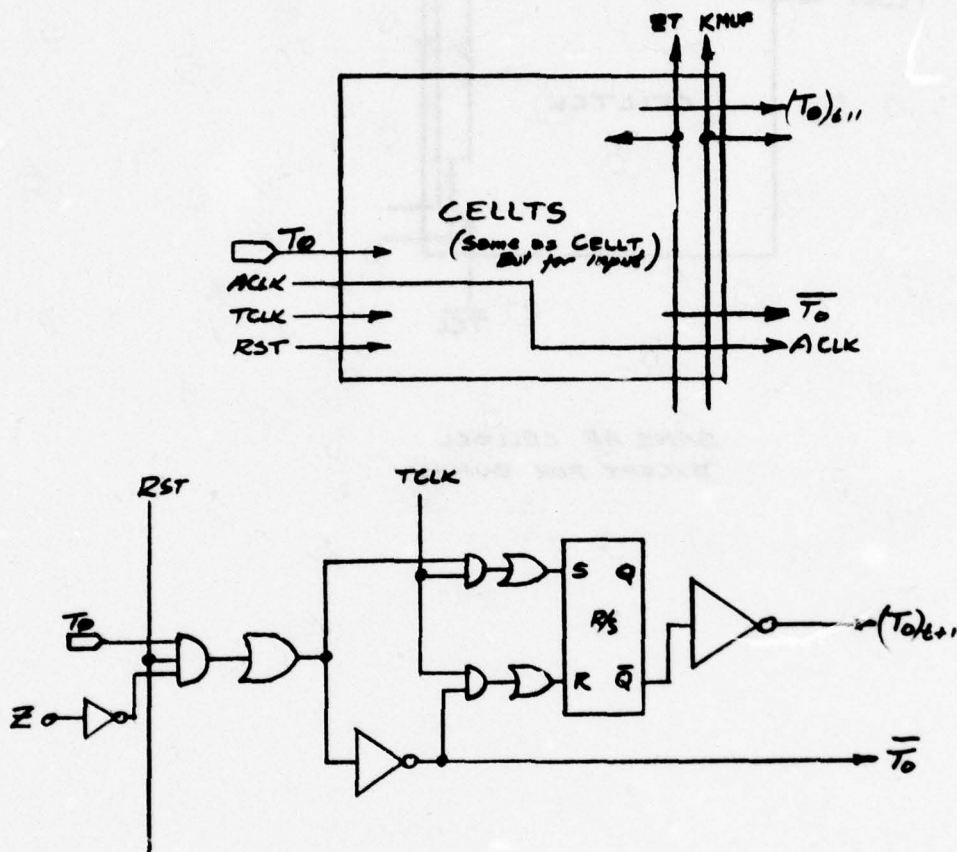
LTR

DESCRIPTION

DATE

APPROVED

20.4 MW.
30 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

MB

MJO

2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLTS

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 64

SCALE

238

SHEET 1 OF

SK

REVISIONS

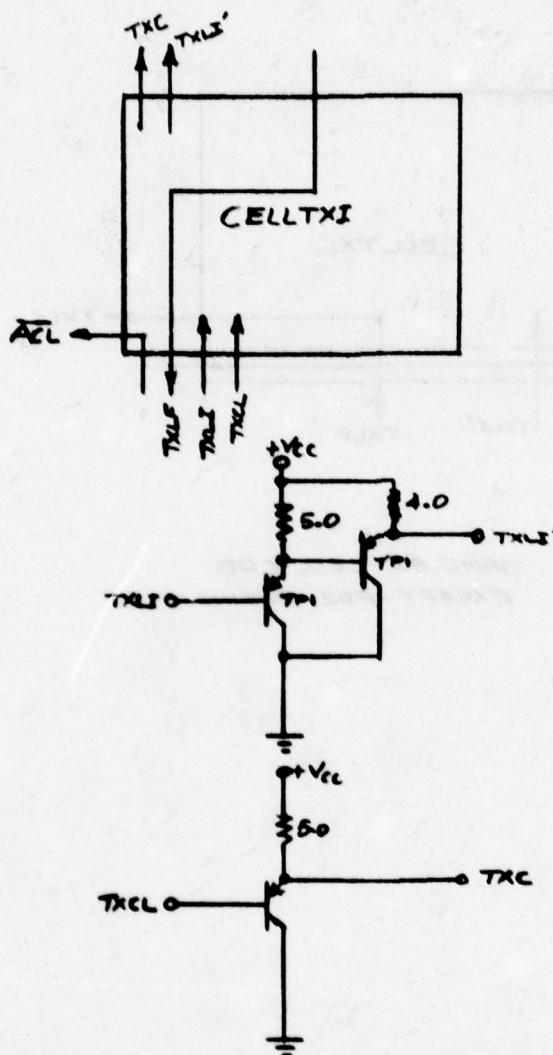
LTR

DESCRIPTION

DATE

APPROVED

2.5 mw.
2 Devices



ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

CELLTXI

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 65

MJO

2849-71

SCALE

239

SHEET 1 OF

SYSTEMS DES REV. 12-71

SK

REVISIONS

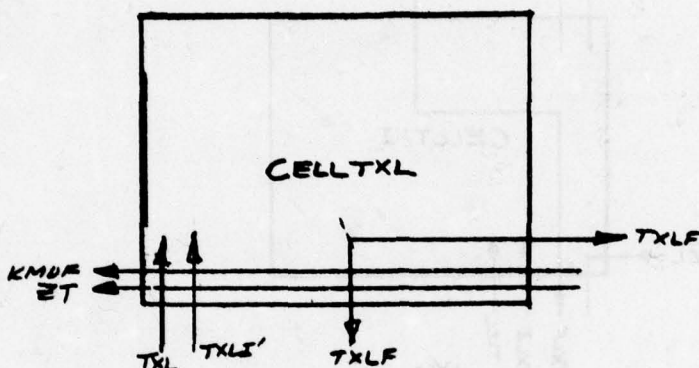
LTR

DESCRIPTION

DATE

APPROVED

32 mw.
36 devices



SAME AS CELL ZDB
EXCEPT FOR BUBBING

ENGINEERING SKETCH

ORIGINATOR

DATE

AMB

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLTXL

SPRU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 66

MJO

2349-71

SCALE

240

SHEET 1 OF

SK

REVISIONS

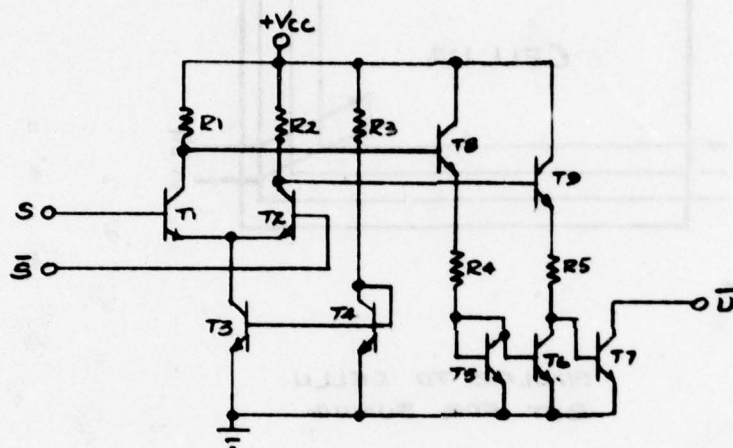
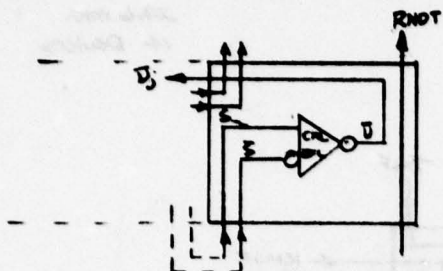
LTR

DESCRIPTION

DATE

APPROVED

24.6 mw.
14 devices



T3-T4 = TNJ
ALL T'S EXCEPT T3-T4 TNN 1

R1 = 1.25
R2 = 1.25
R3 = 3.4
R4 = 2.
R5 = 2.

ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

MJO

2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 67

SCALE

241

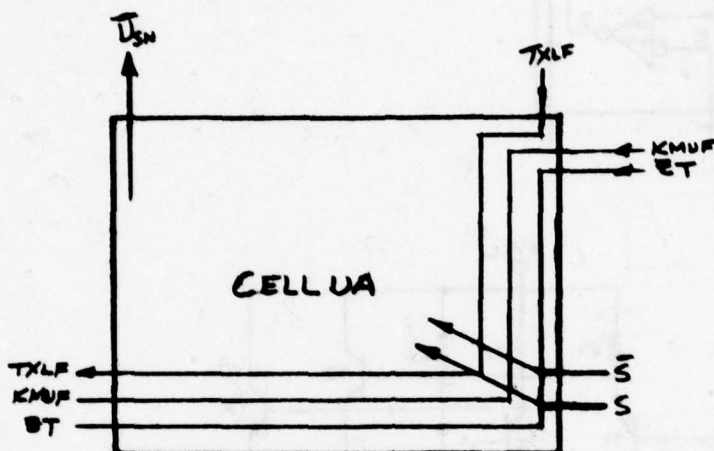
SHEET 1 OF

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
-----	-------------	------	----------

24.6 mm.
14 Devices



SIMILAR TO CELLU
BUT FOR BUSING

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JIB

CELLUA

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 68

MJO

2349-71

SCALE

242

SHEET 1 OF

SK

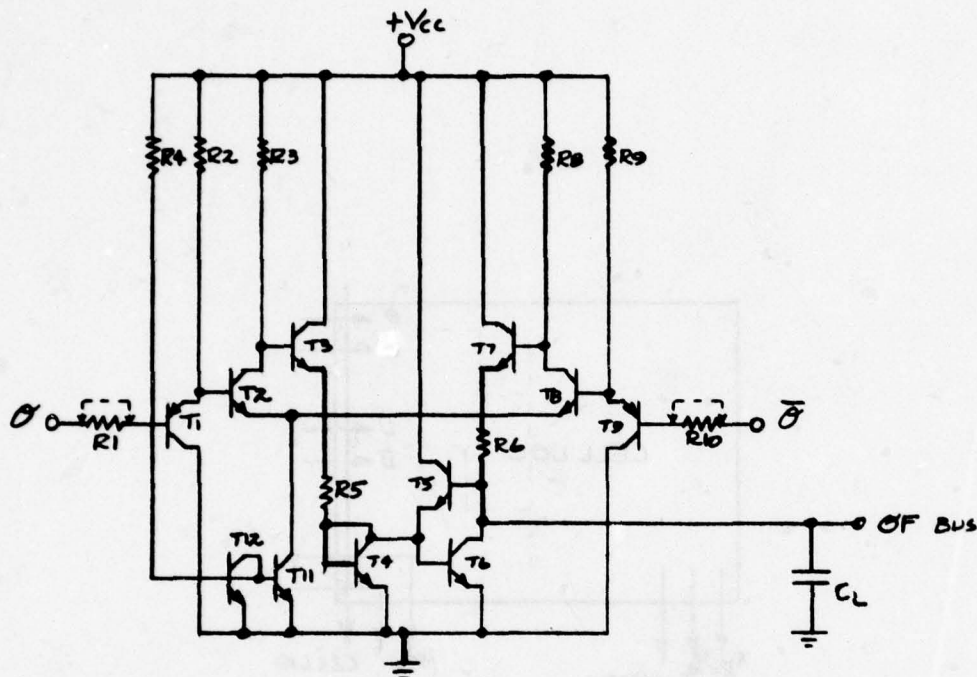
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ALL T'S TNN1 OR TP1
K.A.

R1 = 2.5
R2 = 4.6
R3 = 1.2
R4 = 3.25
R5 = .89
R6 = .89

R1 & R10 Simulate SOURCE
Impedance

R8 = 1.2
R9 = 4.6
R10 = 2.5

Circuit used on

Overflow Bus
Underflow Bus
Sum Bus

CL BUS CAP = 25pf.

SCHEMATIC INCORPORATED IN
CELLUOC
CELLSCC

ENGINEERING SKETCH

ORIGINATOR

DATE

J.B.

MJO

2349-71

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

OVERFLOW CONTROL CKT
SEE CELLUOC
CELLSCC

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 69

SCALE

243

SHEET 1 OF

SK

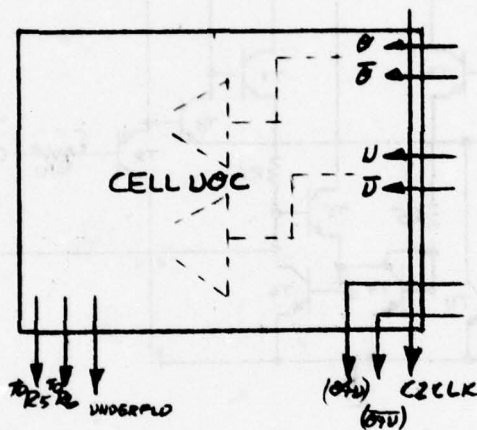
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



TWO DETECTOR CIRCUITS
USED AS PER OVERFLOW
CONTROL CKT.

ENGINEERING SKETCH

ORIGINATOR

DATE

JAB

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLUOC

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 70

MJO

2349-71

SCALE

244

SHEET 1 OF

SK

REVISIONS

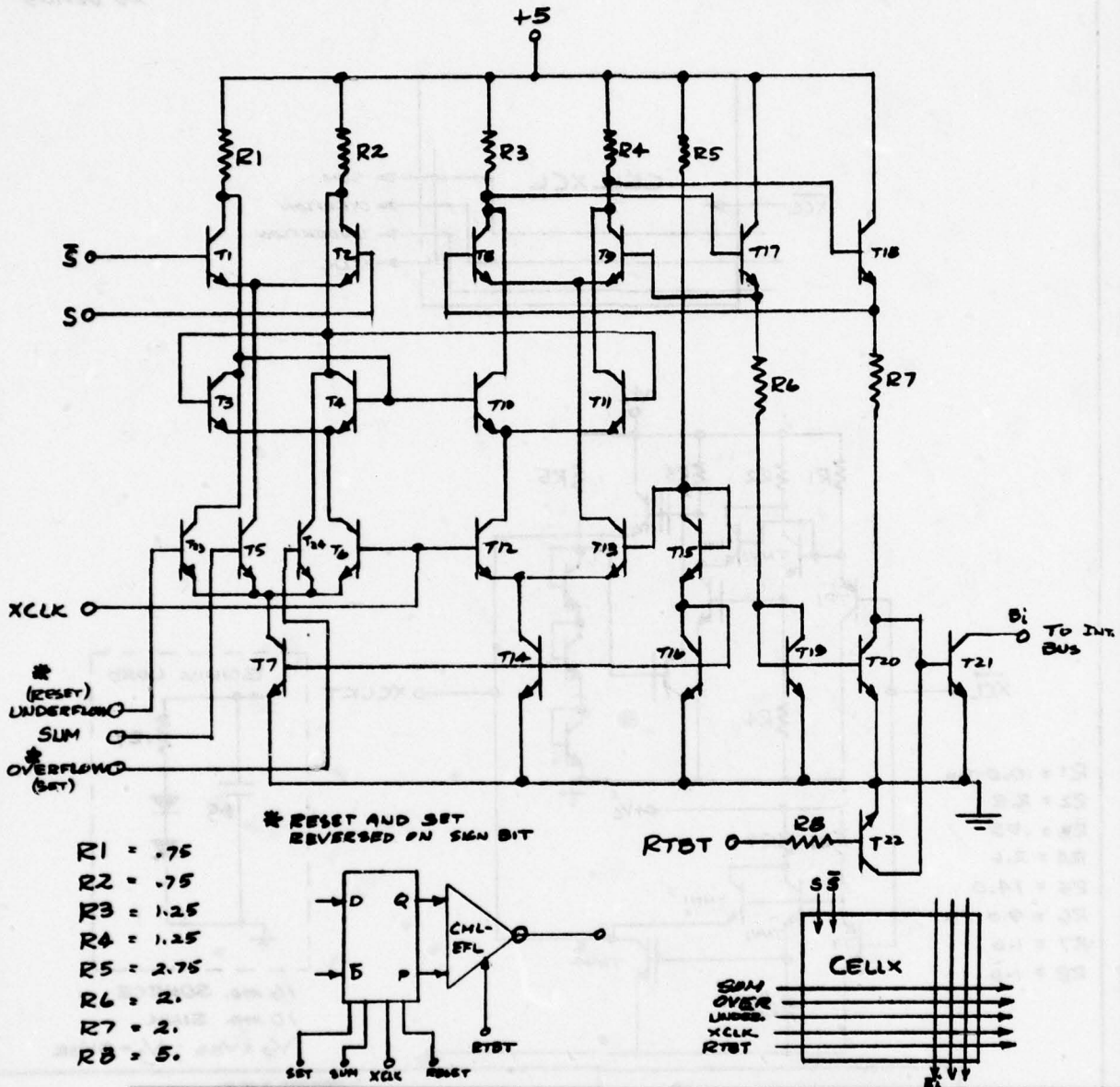
LTR

DESCRIPTION

DATE

APPROVED

20 mw.
32 devices



ENGINEERING SKETCH

ORIGINATOR

DATE

JIB

TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLX

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 71

MJO

2349-71

SCALE

245

SHEET 1 OF

SK

REVISIONS

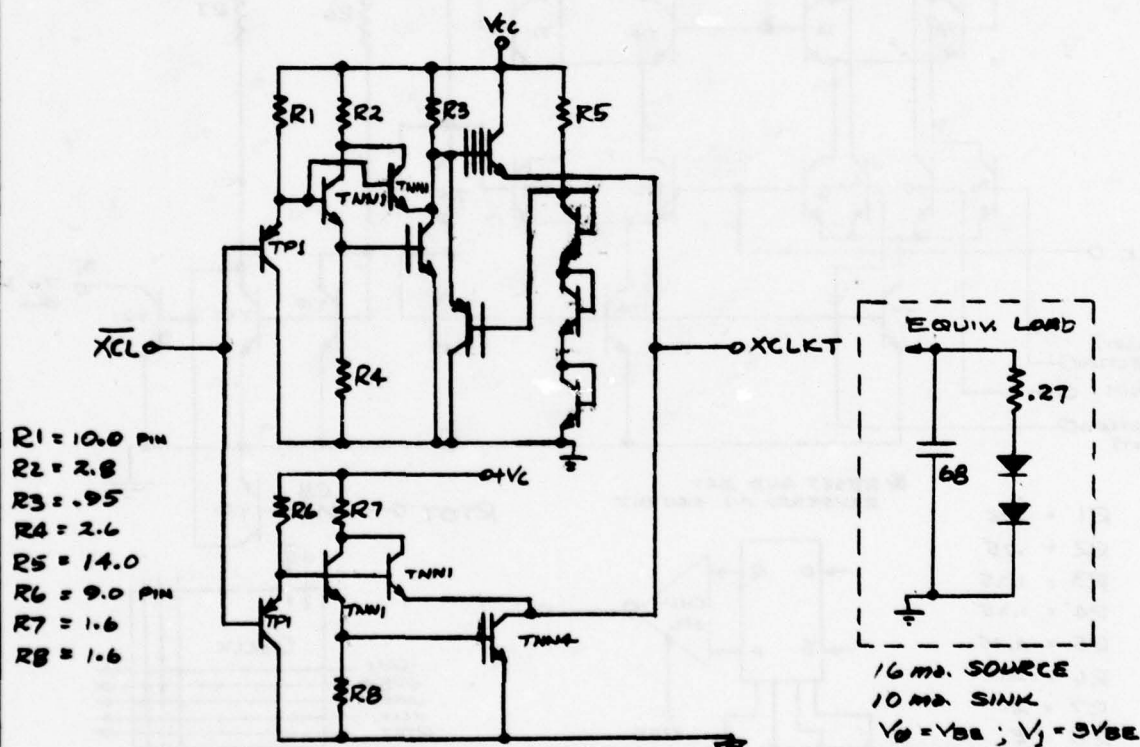
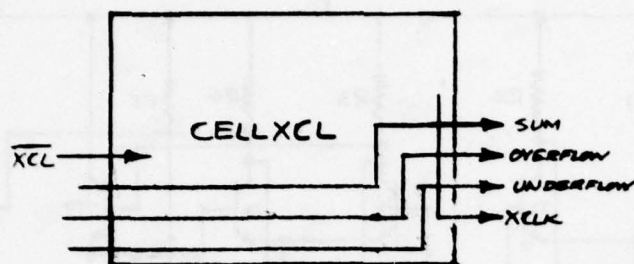
LTR

DESCRIPTION

DATE

APPROVED

37.7 mW.
25 Devices



ENGINEERING SKETCH

ORIGINATOR

DATE

JMB

MJO

2349-71

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

CELLXCL

SPAU

SIZE

CODE IDENT NO.

A

11982

SK

Figure 72

SCALE

246

SHEET 1 OF

SK

REVISIONS

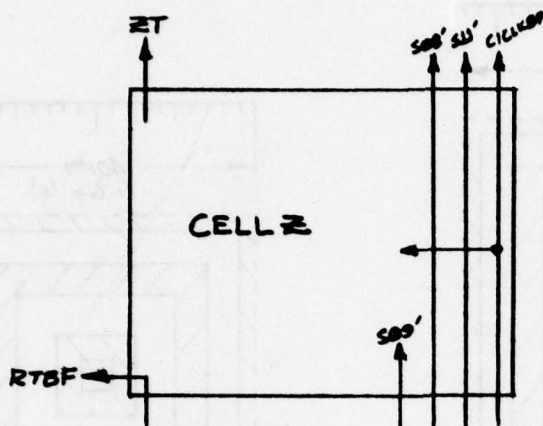
LTR

DESCRIPTION

DATE

APPROVED

32 MW.
36 Devices



SIMILAR TO CELL CDB
BUT FOR PHASE
REVERSAL ON OUTPUT
AND BUS CONNECTIONS.

ENGINEERING SKETCH

ORIGINATOR

DATE

JLB

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDDONO BEACH, CALIFORNIA

CELL 2

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

Figure 73

MJO

2349-71

SCALE

247

SHEET 1 OF

SK

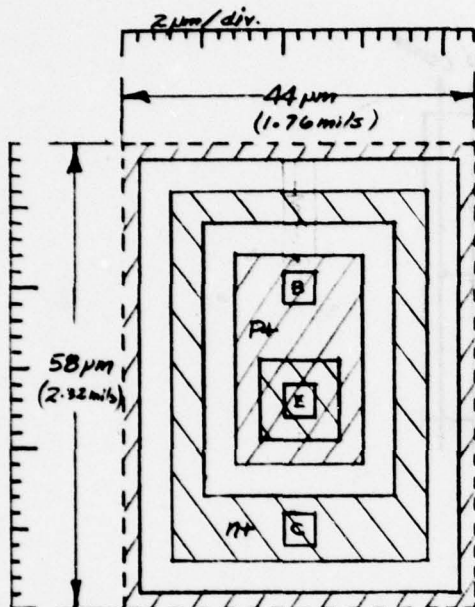
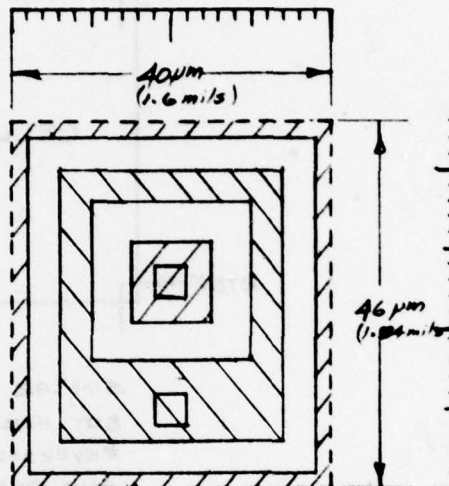
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED

STD. NPN
MODEL TN1STD. PNP
MODEL TP1

ENGINEERING SKETCH

ORIGINATOR

DATE

JLB

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

STD. TRANSISTORS
MODEL TN1
MODEL TP1

SIZE

A

CODE IDENT NO.

11982

SK

FIGURE 74

SCALE

248

SHEET 1 OF

SK

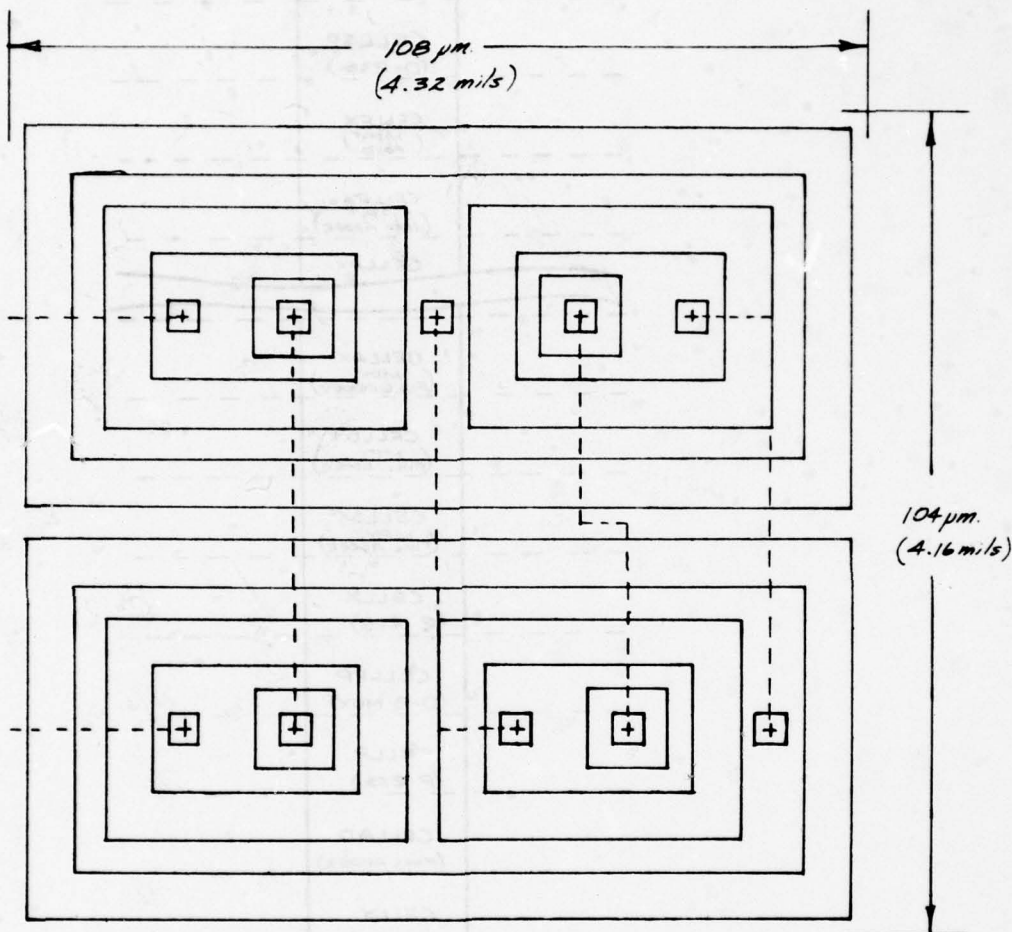
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

ORIGINATOR

JLB

DATE

MJO

TRW

SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

COMPONENT CML

SPAU

SIZE

A

CODE IDENT NO.

11982

SK

FIGURE 75

SCALE

249

SHEET 1 OF

SK

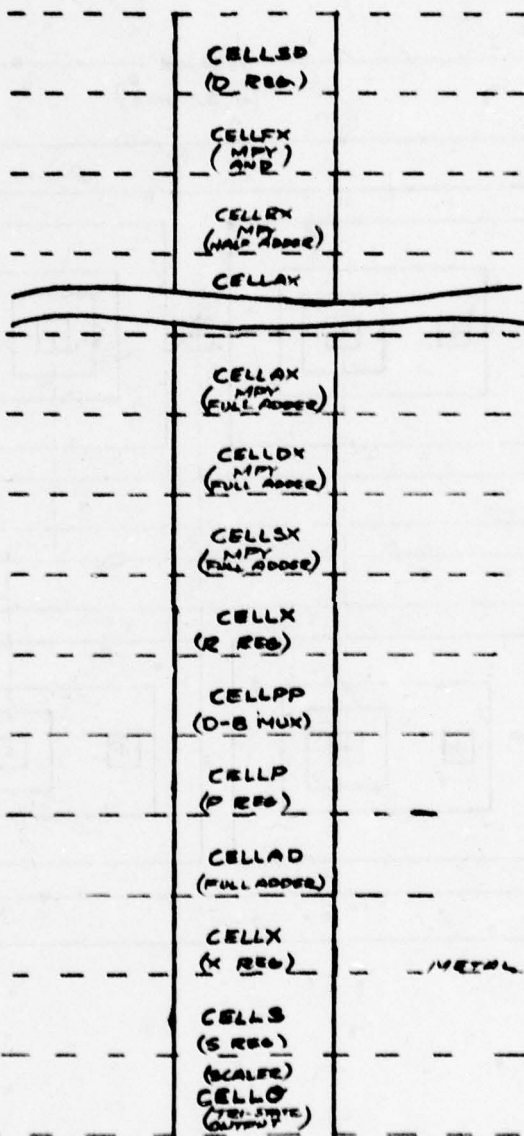
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



ENGINEERING SKETCH

ORIGINATOR

DATE

AIB

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

VERTICAL BIT SLICE THRU SPAU

SIZE

CODE IDENT NO.

A

11982

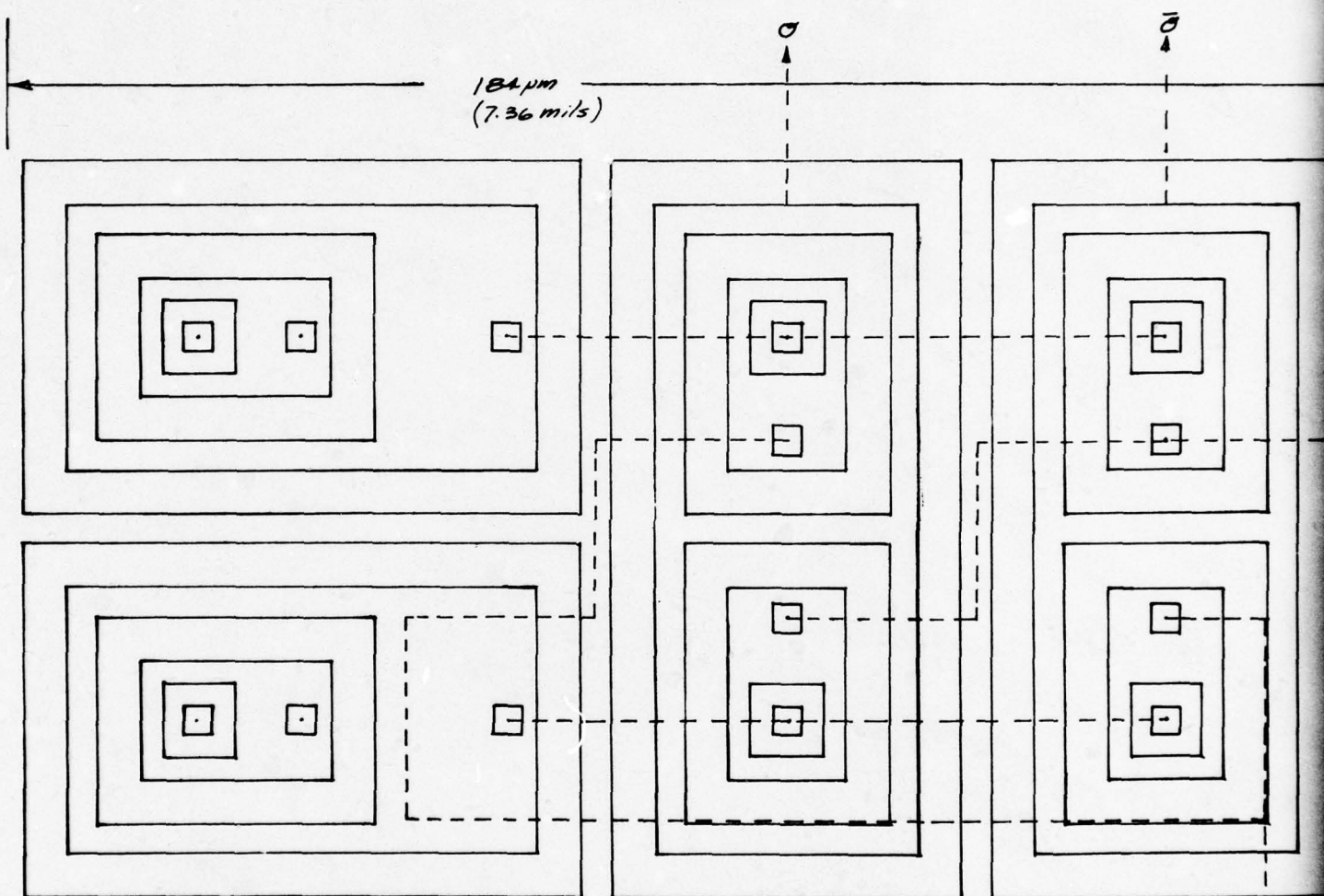
SK FIGURE 76

SCALE

250

SHEET 1 OF

SK



SK

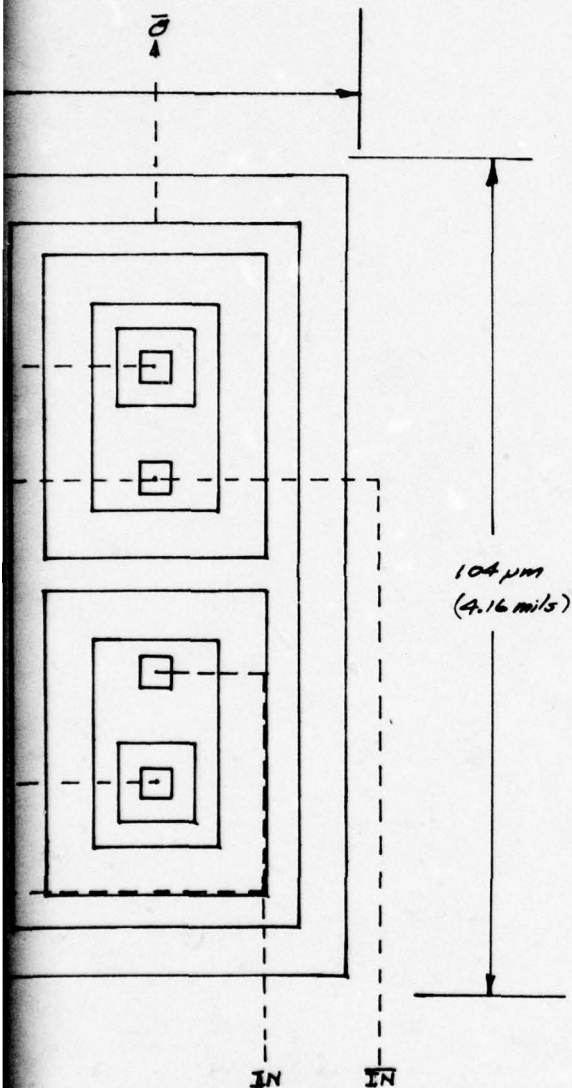
REVISIONS

LTR

DESCRIPTION

DATE

APPROVED



SCALE : 1250X (ORIGINAL DRAWING ONLY)

ENGINEERING SKETCH

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

ORIGINATOR

DATE

JLB

COMPONENT CMLX

SPAU

SIZE

CODE IDENT NO.

B

11982

SK FIGURE 77

MJO

SCALE

251

SHEET 1 OF

SYSTEMS 3663 REV. 12-71

2

TRW

MULTIPLIER-ACCUMULATOR PARALLEL 12-BIT PRELIMINARY

APPENDIX C

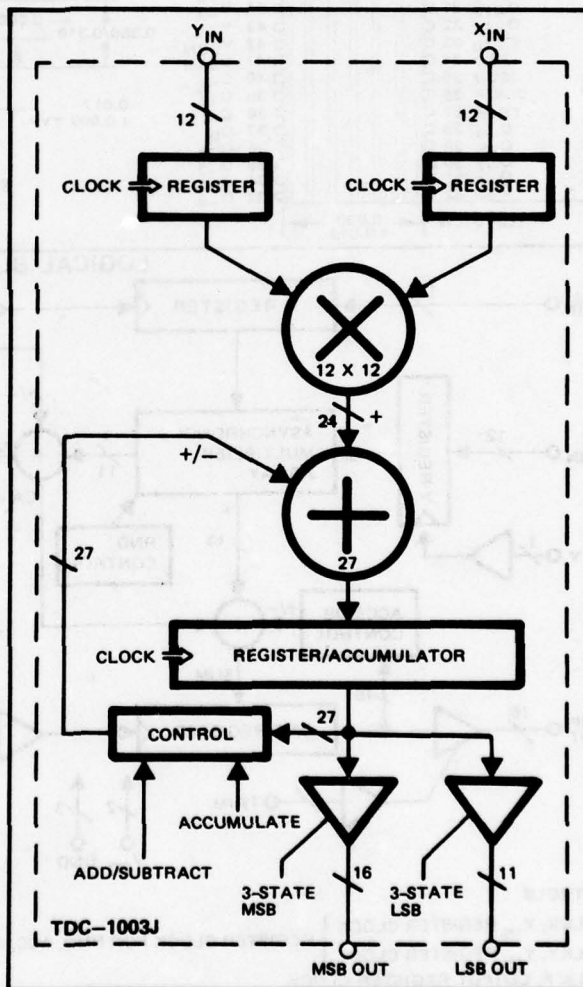
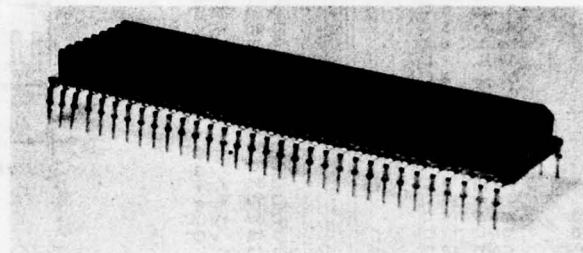
Model: TDC1003J

The TDC1003J is a multifunction arithmetic unit capable of performing 12×12 multiplication as well as product accumulation. It has an additional feature of permitting the accumulator contents to be subtracted from the next product instead of being added, if desired. Input registers are provided in addition to the product accumulation register.

The TDC1003J is directly implementable as the central building block for digital filters, particularly FFTs, for complex multipliers, and for recursive and nonrecursive filter elements.

FEATURES

- 12×12 Bit Parallel, Two's Complement Multiplication
- Controllable Accumulation Either + or -
- 175 nsec Typical Multiply and Accumulate Time
- Much Lower Power/Faster Speed than Equivalent MSI Multiplication-Accumulation Systems
- Round Control
- 27-Bit Accumulation Capacity
- Single Chip, Bipolar Technology
- Asynchronous Mode Multiply
- Radiation Hard
- TTL Input and Output
- Three State Outputs
- Single Power Supply, +5 Volts
- Dual In-Line Package or Flat Pack
- 2.5 Watts Power Consumption



TRW LSI MULTIPLIER-ACCUMULATOR

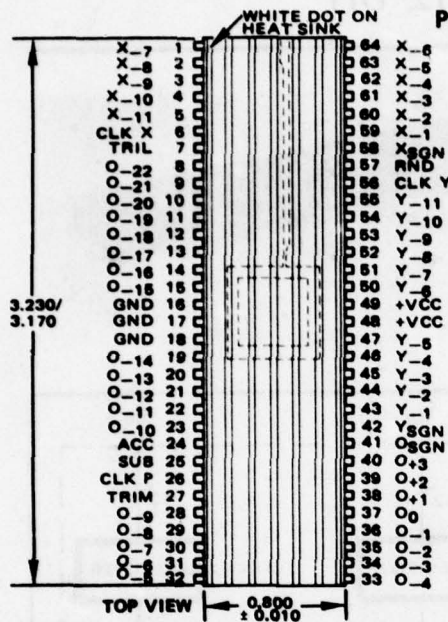
TRW LSI PRODUCTS

ONE SPACE PARK, REDONDO BEACH, CALIFORNIA 90278 (213)535-1831

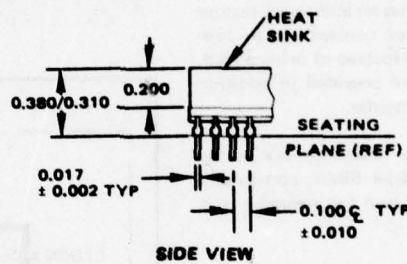
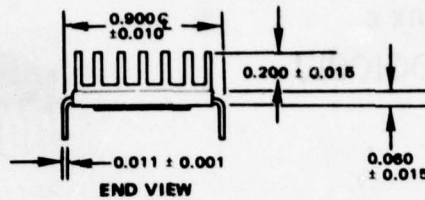
253

8/77

TDC1003J

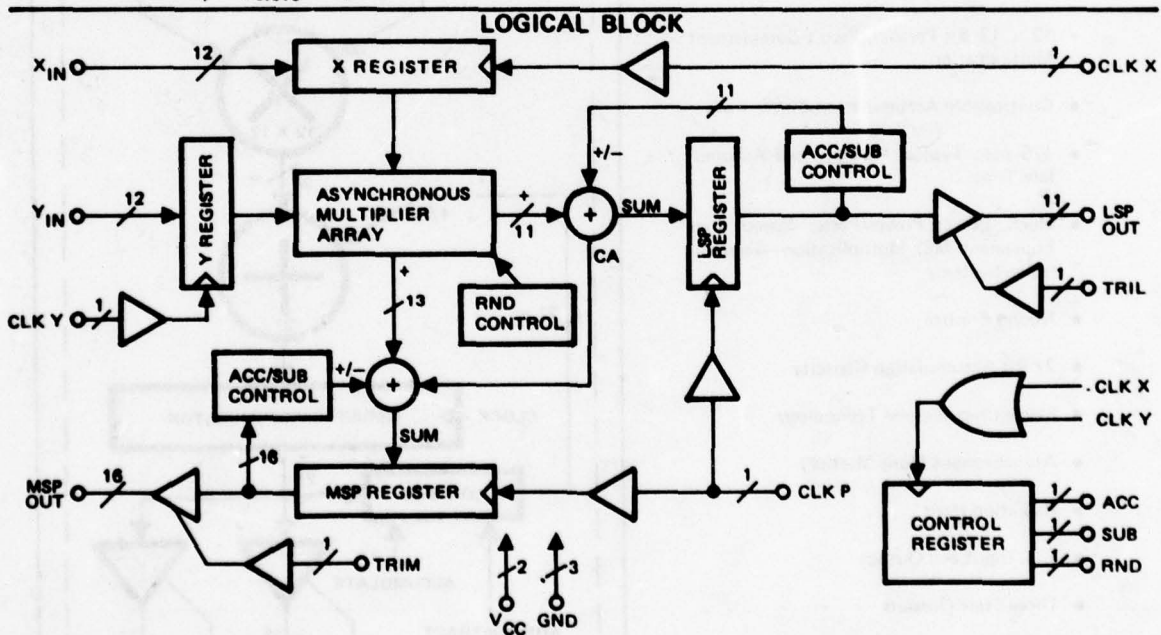


PACKAGE INFORMATION



NOTES:

- DIMENSIONS IN INCHES
- ALL V_{CC} AND GND PINS MUST BE CONNECTED.



CONTROLS

- CLKX, X_{IN} REGISTER CLOCK
- CLKY, Y_{IN} REGISTER CLOCK
- CLK P, OUTPUT REGISTER CLOCK
- TRIL, LSP THREE STATE CONTROL
- TRIM, MSP THREE STATE CONTROL
- RND, ADDS 2⁻¹² TO PRODUCT (FRACTIONAL 2S COMPLEMENT FIELD)
- ACC, ENABLES ACCUMULATOR MODE
- SUB, CONTROLS ADDITION/SUBTRACTION OF ACCUMULATOR CONTENTS

TDC1003J

absolute maximum ratings over operating temperature range

Supply voltage	-0.5 to 7.0 V
Input voltage0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range0°C to 70°C
Storage temperature range	-85°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

recommended operating conditions

	TDC1003			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5.0	5.5	V
Clock pulse width (measured at 1.5 V level)	25			ns
Input register setup time, T_S (see Figure 1)	5			ns
Input register hold time, T_H (see Figure 1)	15			ns
Operating ambient temperature	0		70	°C

electrical characteristics over recommended temperature range

PARAMETER	TEST CONDITIONS	TDC1003			UNIT
		MIN	TYP	MAX	
V_{IH} High-level input voltage		2.0			V
V_{IL} Low-level input voltage				0.8	V
V_{OH} High-level output voltage	$V_{CC} = \text{NOM}$, $I_{OH} = -0.4 \text{ mA}$	2.4	2.7		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 4.0 \text{ mA}$		0.3	0.5	V
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_{IH} = 2.4$		-2	75	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_{IL} = 0.4$		-5	-75	μA
I_{IN} Clocks*	$V_{CC} = \text{MAX}$, $V_{IH} = 2.4$			75	μA
I_{IL} Clocks*	$V_{CC} = \text{MAX}$, $V_{IL} = 0.4$			-0.75	mA
I_{CC} Supply current	$V_{CC} = \text{NOM}$		500	750	mA

At $T_{\text{ambient}} = 25^\circ\text{C}$, $V_{CC} = \text{NOM}$.

* Clock P is two equivalent clock input loads.

switching characteristics, $V_{CC} = 5.0$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multiply accumulate time, input register clock To output register clock, T_{MA}	See Figure 5		150	175	ns
Output delay T_D	Load 1, see Figures 3, 6		40	50	ns
Three state output delay Output enable Output disable	Load 2, see Figures 4, 6 Load 2, see Figures 4, 6		40 30	50 40	ns ns

TDC1003J

12 X 12 BIT PARALLEL MULTIPLIER-ACCUMULATOR

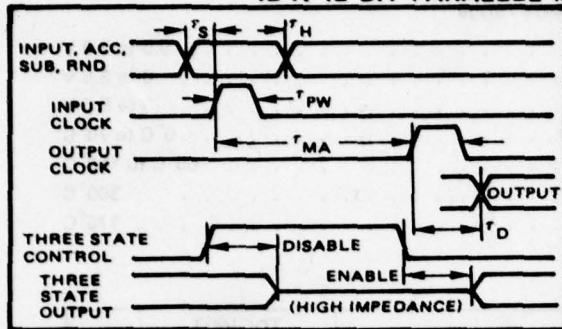


Figure 1. Timing Diagram

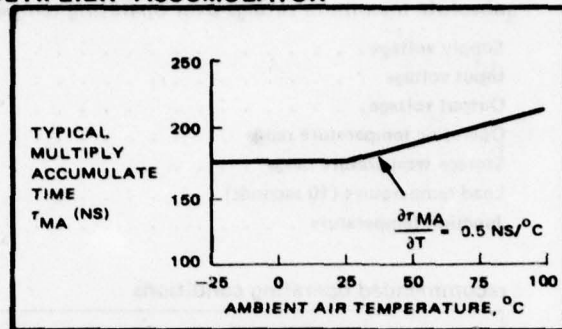


Figure 5. Multiply and Accumulate Time Versus Temperature

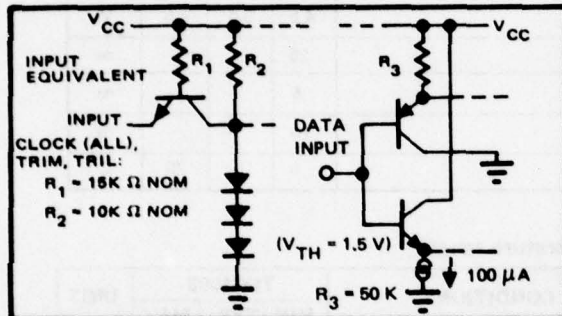


Figure 2. Input Schematics

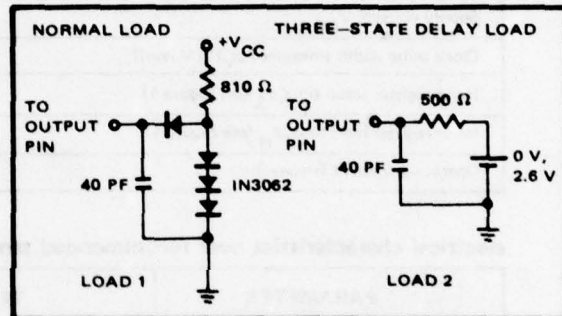


Figure 6. Test Loads for Delay Measurements

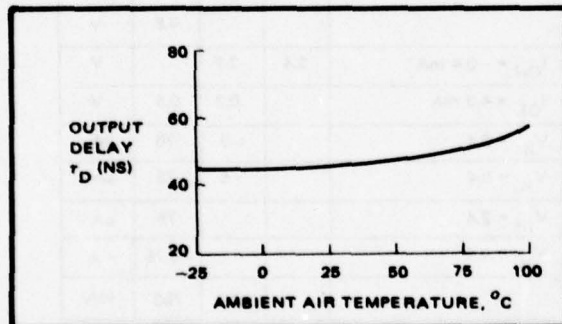


Figure 3. Output Delay Versus Temperature

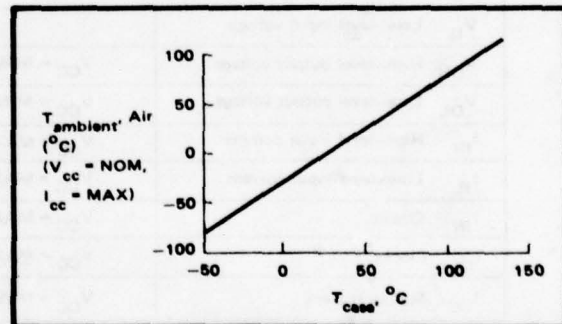


Figure 7. $T_{\text{ambient, Air}}$ Versus T_{case}

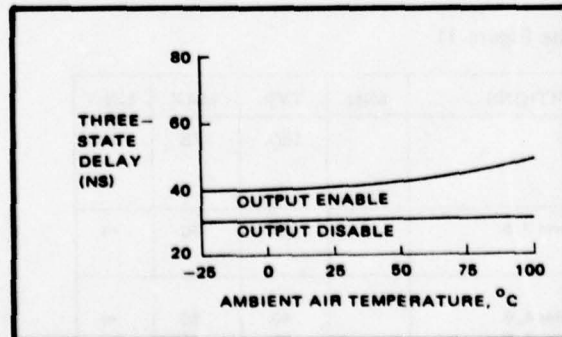


Figure 4. Three State Delay Versus Temperature

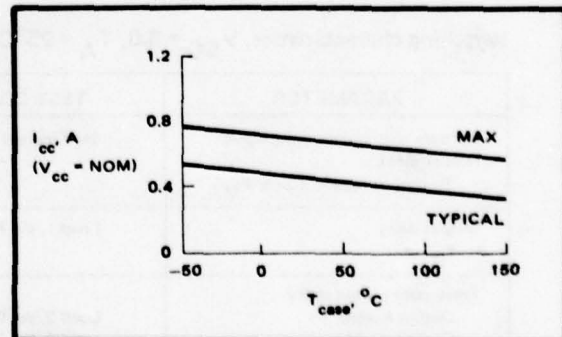


Figure 8. I_{CC} Versus T_{case}

CONTROLS DESCRIPTION: TDC1003J

ACC, SUB, and RND are loaded into registers by either CLKX or CLKY.

ACC: When the ACC signal is low, the next product clocked into the MSP and LSP accumulating registers has zero added to it, i.e., it is the first product in a series to be summed. The ACC signal is then brought high. Subsequent products are then accumulated in the product registers. If accumulation is not desired, the ACC is placed in the low position: the TDC1003J then functions as a standard multiplier.

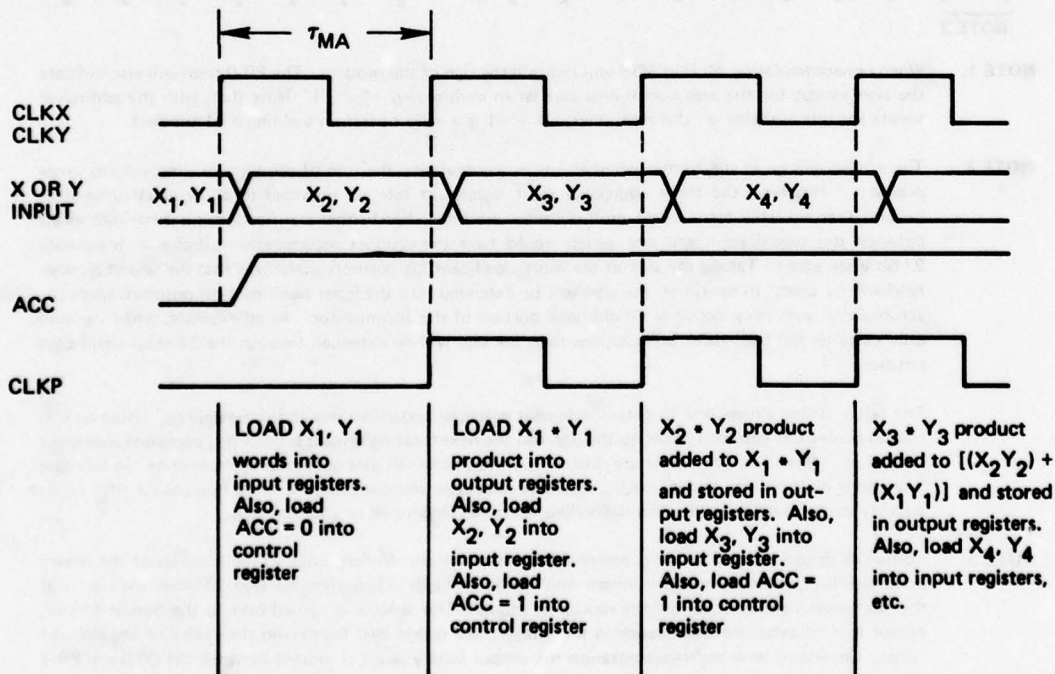
SUB: When the SUB signal is high, the accumulator contents are subtracted from the next product and the difference is then stored in the output registers. When low, the accumulator contents are added to the next product (straight accumulation). The SUB control is enabled by ACC. $SUB' = (SUB \oplus ACC)$.

RND: When RND is high, the quantity 2^{-12} (for fractional 2s complement field, see FORMAT, page 6) is added to the next product.

TRIM, TRIL: Non-registered three state buffer controls: 'O' = enable, 'I' = disable.

TYPICAL OPERATING SEQUENCE

SUM OF PRODUCTS



- NOTES:**
1. SUB = 0 for sequence above.
 2. X_n, Y_n are 12-Bit Two's Complement Numbers.

TDC1003J

FORMAT: 2'S COMPLEMENT FRACTIONAL NOTATION (NOTE 3)

X INPUT	X _{SGN}	X ₋₁	X ₋₂	X ₋₃	X ₋₄	X ₋₅	X ₋₆	X ₋₇	X ₋₈	X ₋₉	X ₋₁₀	X ₋₁₁
	SGN	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹

Y INPUT	Y _{SGN}	Y ₋₁	Y ₋₂	Y ₋₃	Y ₋₄	Y ₋₅	Y ₋₆	Y ₋₇	Y ₋₈	Y ₋₉	Y ₋₁₀	Y ₋₁₁
---------	------------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	------------------	------------------

OUTPUT FORMAT WHEN NONACCUMULATING PRODUCTS (ACC = 0) FOR PINOUT DIAGRAM O_n = PR_n

PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR	PR
SGN	SGN	SGN	SGN	0	-1	-2	-3	-4	-5	-16	-17	-18	-19	-20	-21	-22
2 ⁻⁴	2 ⁻³	2 ⁻²	2 ⁻¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	2 ⁻²¹	2 ⁻²²
SGN	SGN	SGN	SGN													

NOTE 1

OUTPUT FORMAT WHEN ACCUMULATING PRODUCTS (ACC = 1) FOR PINOUT DIAGRAM O_n = S_n

SUM	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
SGN	+4	+3	+2	+1	0	-1	-2	-3	-4	-5	-16	-17	-18	-19	-20	-21	-22
SGN	2^{-4}	2^{-3}	2^{-2}	2^{-1}	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}
NOTE 2																	

NOTE 2

NOTE 1. When nonaccumulating, all four MSB will indicate the sign of the product. The PR-0 term will also indicate the sign except for the one exceptional case when multiplying -1×-1 . Note that, with the additional significant bits available on this multiplier, -1×-1 is a valid operation yielding a +1 product.

NOTE 2. There is no change in the format whether one is accumulating the sum of products or simply doing single products. However, the three additional most significant bits are provided to allow valid summation beyond that available for a single multiplication product. For further clarification, no difference exists between this organization and one which would have the product accumulation off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position guarantees that the largest number field will be used. In operation the sign will be extended into the lesser significant bit positions when the accumulated sum only occupies a right-hand portion of the accumulator. As an example, when the sum only occupies the least three bit positions then the sign will be extended through the 24 most significant positions.

The latter factor allows one to detect imminent overflow/underflow should this be desired. Using an off-chip exclusive-OR gate connected to the sign and the next most significant bit will flag imminent overflow/underflow. When the two inputs are different, the exclusive-OR gate goes to a logic one state. In this case four more multiply-accumulate cycles would be allowable without overflow/underflow, but a fifth could possibly cause overflow/underflow depending upon the magnitude of the sum steps.

NOTE 3. Format is shown using a 2's complement fractional notation. In this notation the location of the binary point signifying separation of the integer and fractional fields is just after the sign, between the sign and the next most significant bit for the multiplier inputs. This scheme is carried over to the output format, except that an extended significance to the integer field is provided (to extend the utility of the accumulator). Consistent with the input notation the output binary point is located between the PR-0 and PR-1 bit positions (for the nonaccumulate mode). For the accumulate mode the binary point position is the same between the S+0 and S-1 bit positions.

It is arbitrary where the binary point is considered located as long as one is consistent with both input and output formats. One can consider the number field entirely integer, i.e., with the binary point just to the right of the least significant bit for input, product, and accumulated sum.

TYPICAL APPLICATIONS OF TDC1003J

DIGITAL FILTER FOR NUMERICAL INTEGRATION OF SAMPLED DATA

Based on the area under a parabolic arc, Simpson's rule is an accepted method for numerical integration of a sampled data sequence.

Let a function $y(t)$ be sampled at $n + 1$ points, such that y_0, y_1, \dots, y_n are equally spaced at an incremental interval T . Assume that n is even. Then according to Simpson's rule (see almost any calculus textbook), the area A_S under the curve $y(t)$, given by

$$A_S = \int_{t_1}^{t_1 + nT} y(t) dt, \quad (1)$$

may be approximated by

$$A_S = \frac{T}{3} (y_0 + 4y_1 + 2y_2 + 4y_3 + 2y_4 + \dots + 4y_{n-1} + y_n). \quad (2)$$

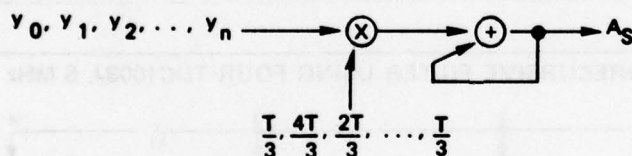
This is generally more accurate than the so-called trapezoidal rule

$$A_T = \frac{T}{2} (y_0 + 2y_1 + 2y_2 + \dots + 2y_{n-1} + y_n), \quad (3)$$

which approximates the function $y(t)$ by straight-line segments and therefore fails to take account of curvature.

An accumulation of the terms in Equation (2), therefore, implements Simpson's rule explicitly, where it is necessary only to input the sequence of sampled points and the appropriate sequence of weighing coefficients. After any step m , where $m < n$, the contents of the accumulator are \tilde{A}_m , which is an approximation to the running integral up to that point. When $m = n$ and the accumulation is terminated with the proper weighting coefficient (see Note), the evaluation is complete and $\tilde{A}_n = A_S$.

BLOCK DIAGRAM (Uses one TDC 1003J)

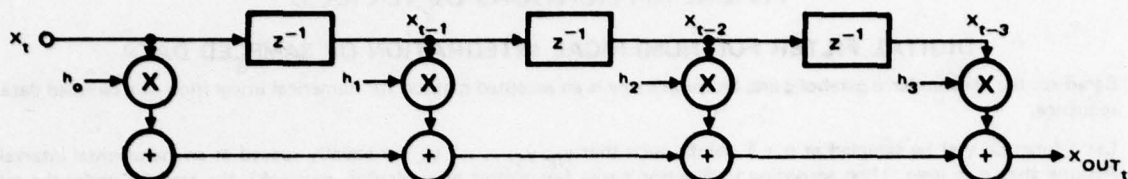


Operation Sequence					Contents of Output Registers At End of Operation	Cumulative Time at Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	$y_0 \cdot \frac{T}{3}$	0	0	0	$y_0 \cdot \frac{T}{3} = \tilde{A}_1$	200
2	$y_1 \cdot \frac{4T}{3}$	1	0	0	$\tilde{A}_1 + y_1 \cdot \frac{4T}{3} = \tilde{A}_2$	400
3	$y_2 \cdot \frac{2T}{3}$	1	0	0	$\tilde{A}_2 + y_2 \cdot \frac{2T}{3} = \tilde{A}_3$	600
4	$y_3 \cdot \frac{4T}{3}$	1	0	0	$\tilde{A}_3 + y_3 \cdot \frac{4T}{3} = \tilde{A}_4$	800

NOTE: To avoid termination error, based on Simpson's rule outlined above, the integration should terminate on an odd number of samples (n even) with a weight of $T/3$, as shown. If it is necessary to terminate on an even number of samples (n odd), then it is a good approximation to keep the sequence up to that point and terminate with a weight of $2T/3$.

TDC1003J

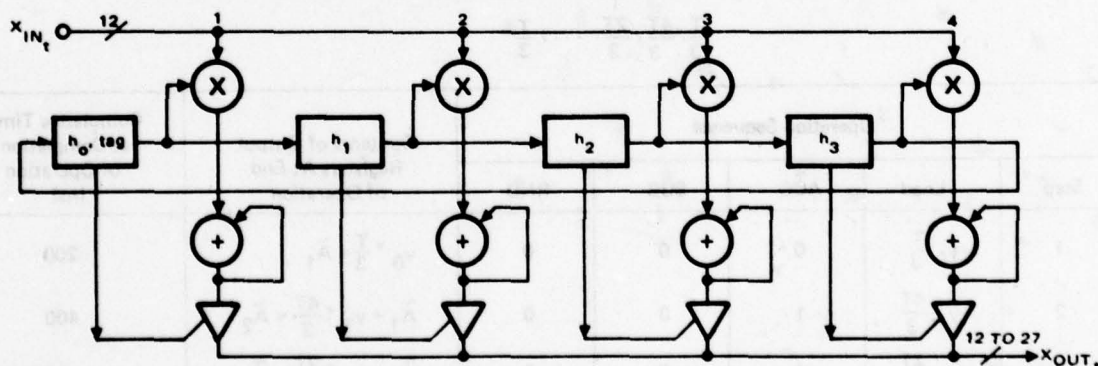
NONRECURSIVE FILTER



Using one TDC1003J in time sequenced operation.

Operation Sequence					Contents of Output Registers at Completion of Operation	Cumulative Time At Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	X_t, h_0	0	0	0	$X_t * h_0$	200
2	X_{t-1}, h_1	1	0	0	$X_t * h_0 + X_{t-1} * h_1$	400
3	X_{t-2}, h_2	1	0	0	$X_t * h_0 + X_{t-1} * h_1 + X_{t-2} * h_2$	600
4	X_{t-3}, h_3	1	0	0	$X_t * h_0 + X_{t-1} * h_1 + X_{t-2} * h_2 + X_{t-3} * h_3 = X_{OUT,t}$	800 cycle complete
5	X_{t+1}, h_0	0	0	0	$X_{t+1} * h_0$	1000
6	X_t, h_1	1	0	0	$X_{t+1} * h_0 + X_t * h_1$	1200
7	X_{t-1}, h_2	1	0	0	$X_{t+1} * h_0 + X_t * h_1 + X_{t-1} * h_2$	1400
8	X_{t-2}, h_3	1	0	0	$X_{t+1} * h_0 + X_t * h_1 + X_{t-1} * h_2 + X_{t-2} * h_3 = X_{OUT,t+1}$	1600 cycle complete

PIPELINED NONRECURSIVE FILTER USING FOUR TDC1003J, 5 MHz

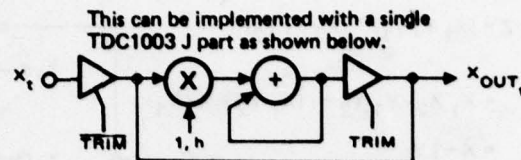
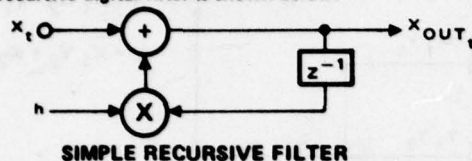


In this method, four TDC1003J parts are used in a parallel-out kind of connection. An external four-stage circulating shift register holds the weighting functions, h . A tag bit is also circulated in the h shift registers which operates the 3-state control, thereby busing the accumulator contents to the output in sequence. Input register clocking, output register clocking and h shift register are all operated directly from the 5 MHz system clock. The control ACC is also operated from the tag bit as well as the 3-state control. As can be traced from the block diagram, each TDC1003J accumulates four products and then is gated to the output bus. On the next clock period the adjacent TDC1003J is outputted, etc. By these means, steady outputs at the 5 MHz rate are sustained. The latency period is four clock periods or 800 ns. The internal operation sequence for any one TDC1003J is the same as shown in the previous implementation.

TDC1003J

RECURSIVE DIGITAL FILTER IMPLEMENTED WITH TDC1003

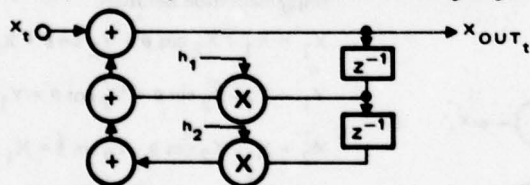
The usual block diagram for the simplest recursive digital filter is shown below.



In this case, two-step operation is used where the operand into the multiplier is alternated between 1 and h and the output is read out on alternate clock cycles. Operation is shown below, assuming initial output accumulator contents of value v.

Operation Sequence						Contents of Output Registers at Completion of Operation	Cumulative Time of Completion of Operation
Step	Load	ACC	SUB	RND	TRIM		
	Initial state t_0					$X_{OUT_{t_0}} = v$	0
1	$X_{OUT_{t_0}} \cdot h$	1	0	0	0	hv	200
2	$X_{t+1} \cdot 1$	1	0	0	1	$X_{OUT_{t+1}} = X_{t+1} + hv$ (read out to destination)	400 Cycle complete
3	$X_{OUT_{t+1}} \cdot h$	1	0	0	0	$h(X_{t+1} + hv)$	600
4	$X_{t+2} \cdot 1$	1	0	0	1	$X_{OUT_{t+2}} = X_{t+2} + h(X_{t+1} + hv)$ (read out to destination)	800 Cycle complete

For a two or more pole filter we have the following diagram:



$$X_{OUT_{t_0}} = v$$

$$X_{OUT_{t+1}} = X_{t+1} + h_1 v$$

$$X_{OUT_{t+2}} = X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v$$

$$X_{OUT_{t+3}} = X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v] + h_2 (X_{t+1} + h_1 v)$$

$$X_{OUT_{t+4}} = X_{t+4} + h_1 X_{t+3} + h_1 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v] + h_2 (X_{t+1} + h_1 v) + h_2 [X_{t+2} + h_1 (X_{t+1} + h_1 v) + h_2 v]$$

In general

$$X_{OUT_t} = X_t + h_1 (X_{OUT_{t-1}}) + h_2 (X_{OUT_{t-2}}) + \dots + h_n (X_{OUT_{t-n}})$$

$$X_{OUT_t} = X_t + \sum_{i=1}^n h_i (X_{OUT_{t-i}})$$

Using the methods shown for the other example, the two pole filter can be stepped at 600 ns intervals using one TDC1003.

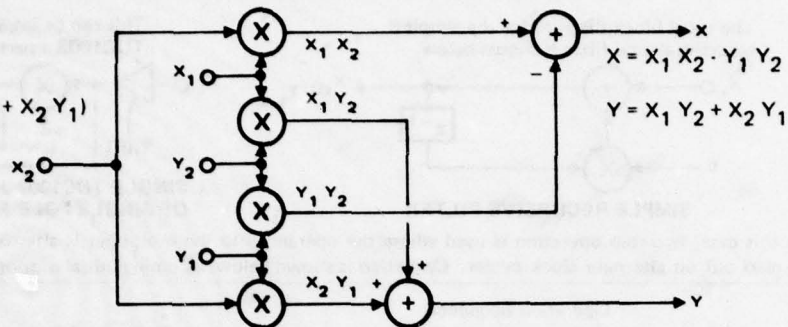
TDC1003J

COMPLEX MULTIPLICATION

$$Z = (X_1 + jY_1) * (X_2 + jY_2)$$

$$= X_1 X_2 - Y_1 Y_2 + j(X_1 Y_2 + X_2 Y_1)$$

$$= X + jY$$



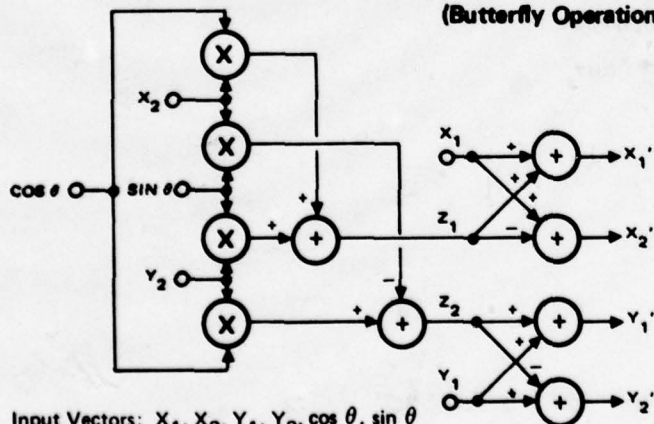
Using one TDC1003J in time sequenced operation.

Operation Sequence					Contents of Output Registers at Completion of Operation	Cumulative Time at Completion of Operation (ns)
Step	Load	ACC	SUB	RND		
1	Y_1, Y_2	0	0	0	$Y_1 * Y_2$	200
2	X_1, X_2	1	1	0	$X_1 * X_2 - Y_1 * Y_2 = X$ (transfer to destination)	400
3	X_1, Y_2	0	0	0	$X_1 * Y_2$	600
4	X_2, Y_1	1	0	0	$X_1 * Y_2 + X_2 * Y_1 = Y$ (transfer to destination)	800

Using two TDC1003s, it is obvious that the above complex multiplication can be performed in 400 nsec.

FFT DECIMATION-IN-TIME KERNEL SEQUENCE

(Butterfly Operation)



Input Vectors: $X_1, X_2, Y_1, Y_2, \cos \theta, \sin \theta$

Principal Equations:

$$F_K = \sum_{n=0}^{N-1} f_n w^{nK}, K = 0, 1, 2, \dots, N-1,$$

$$w \equiv e^{-j2\pi/N}$$

$$w^K \equiv e^{-j2\pi K/N} = e^{-j\theta} = \cos \theta - j \sin \theta$$

Implementation Solution:

$$X_1' = X_1 + X_2 \cos \theta + Y_2 \sin \theta = X_1 + Z_1$$

$$Y_1' = Y_1 - X_2 \sin \theta + Y_2 \cos \theta = Y_1 + Z_2$$

$$X_2' = X_1 - X_2 \cos \theta - Y_2 \sin \theta = X_1 - Z_1$$

$$Y_2' = Y_1 + X_2 \sin \theta - Y_2 \cos \theta = Y_1 - Z_2$$

FFT points represented by

$$X_1 + jY_1, X_2 + jY_2$$

Transformed Vectors

$$X_1', X_2', Y_1', Y_2'$$

$$\theta \equiv 2\pi K/N$$

$$Z_1 \equiv X_2 \cos \theta + Y_2 \sin \theta$$

$$Z_2 \equiv -X_2 \sin \theta + Y_2 \cos \theta$$

FFT DECIMATION-IN-TIME KERNEL SEQUENCE (CONTINUED)

Using one TDC1033J in time sequence operation.

Operation Sequence					Contents of Output Registers at Completion of Operation (Note 1)	Cumulative Time at Completion of Operation (ns) (Note 3)
Step	Load/Hold (L/H)	ACC	SUB	RND		
1	L $X_2, \cos \theta$	0	0	0	$X_2 \cos \theta$	200
2	L $Y_2, \sin \theta$	1	0	0	$X_2 \cos \theta + Y_2 \sin \theta = Z_1$	400
3	L $X_1, 1$ (Note 4)	1	0	0	$X_1 + Z_1 = X_1'$ (transfer to destination)	600
4	H $X_1, 1$ (Note 2)	1	1	0	$-Z_1$	800
5	H $X_1, 1$	1	0	0	$X_1 - Z_1 = X_2'$ (transfer to destination)	1000
6	L $X_2, \sin \theta$	0	0	0	$X_2 \sin \theta$	1200
7	L $Y_2, \cos \theta$	1	1	0	$-X_2 \sin \theta + Y_2 \cos \theta = Z_2$	1400
8	L $Y_1, 1$	1	0	0	$Y_1 + Z_2 = Y_1'$ (transfer to destination)	1600
9	H $Y_1, 1$	1	1	0	$-Z_2$	1800
10	H $Y_1, 1$	1	0	0	$Y_1 - Z_2 = Y_2'$ (transfer to destination)	2000

Note 1. The outputs are stable within τ_D time after clocking the output registers, typically 30 ns. Outputs are held stable until the next step in the sequence is clocked at the end of the step. Consequently output contents are available to bus to the destination for $\tau_m - \tau_D$ period, approximately 170 ns for $\tau_m = 200$ ns.

Note 2. At steps 4 and 9, if the constant loaded is +2 instead of +1, the above sequence can be shortened by two steps or to 1600 ns. Some loss in accuracy may result using this shortened sequence since the number field would have to include +2 and a quantity such as $\cos \theta$ could only be represented with one less significant binary bit.

Note 3. Using two TDC1003J parts instead of one will allow the kernel operation in one-half the time given above.

Note 4. The absence of a true +1 in the fractional 2s complement number field causes a small error to be introduced. An alternative is to arrange the algorithm so that -1 is used as the operator since this is a valid 2s complement number having unity absolute value. Another alternative which avoids the error is to use a one bit integer field with $\sin \theta$ and $\cos \theta$ scaled accordingly.

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APPENDIX D

SPAU 2 CIRCUIT CELLS

The circuit cell layout for SPAU 2 is shown in Figure 3.4.5 of the main report text. Most of the central core of cells used for the multiplier are the same as used for SPAU 1 and displayed in Appendix B. In this appendix only the unique cells are shown.

Figure 1 shows the circuit schematics used for the Input Cells, INXD, INYD, RND, ACC, and SUB. The major change over the SPAU 1 input cells was to place a buffer amplifier on the input. This placed a fixed delay into the input to compensate for the clock buffer delay and thereby create a near zero setup time for the input registers.

Figure 2 shows new clock buffers and intermediate power drivers. These have much improved speed over the former used in SPAU 1. The power OR driver is unique. The output is push-pull and drives a control line 3/4 around the chip in 5 ns.

Figure 3 shows the circuit cell for LSB logic 1 injection for 2's complement arithmetic. This is standard TTL which interface with the gate.

Figure 4 shows the output cell schematics. These are modified for an improved mirror circuit making the logic translation from CML to TTL.

Figure 5 shows the output register along with the accumulation controls and feed-back to the adder. This operates totally using CML. The adder feed-back couples to EFL circuits directly.

The layout of these cells producing the SPAU 2 drawing was accomplished using Applicon software and computer. The method is basically custom design; however, a standardized cell size was used. The cell size accommodates the largest cell. In some places space utilization could be much improved; however, the high yield 3D process places no particular need to reduce chip size. Approximate space utilization can be seen from the chip photograph in the text, Figure 3.4.6.

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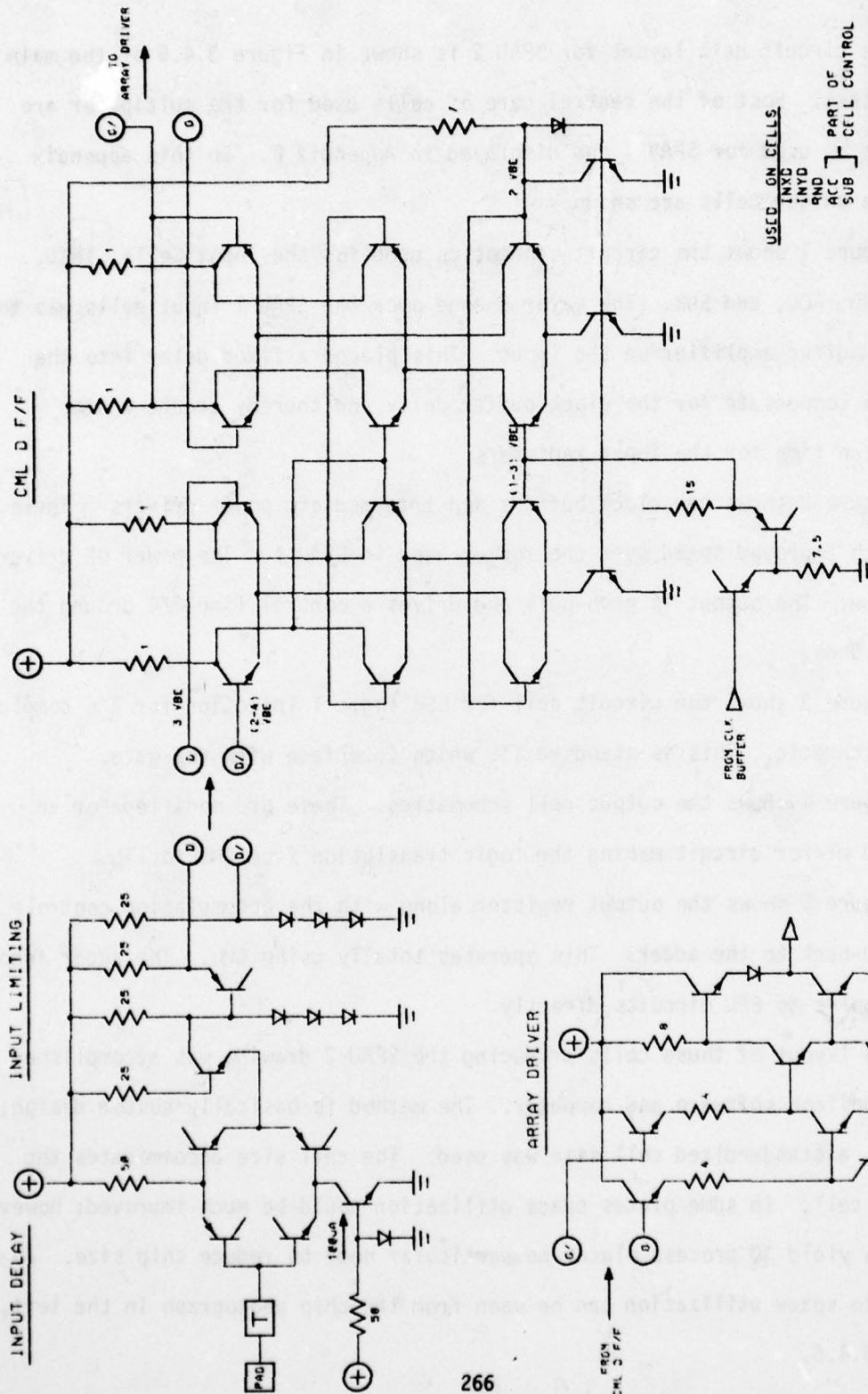
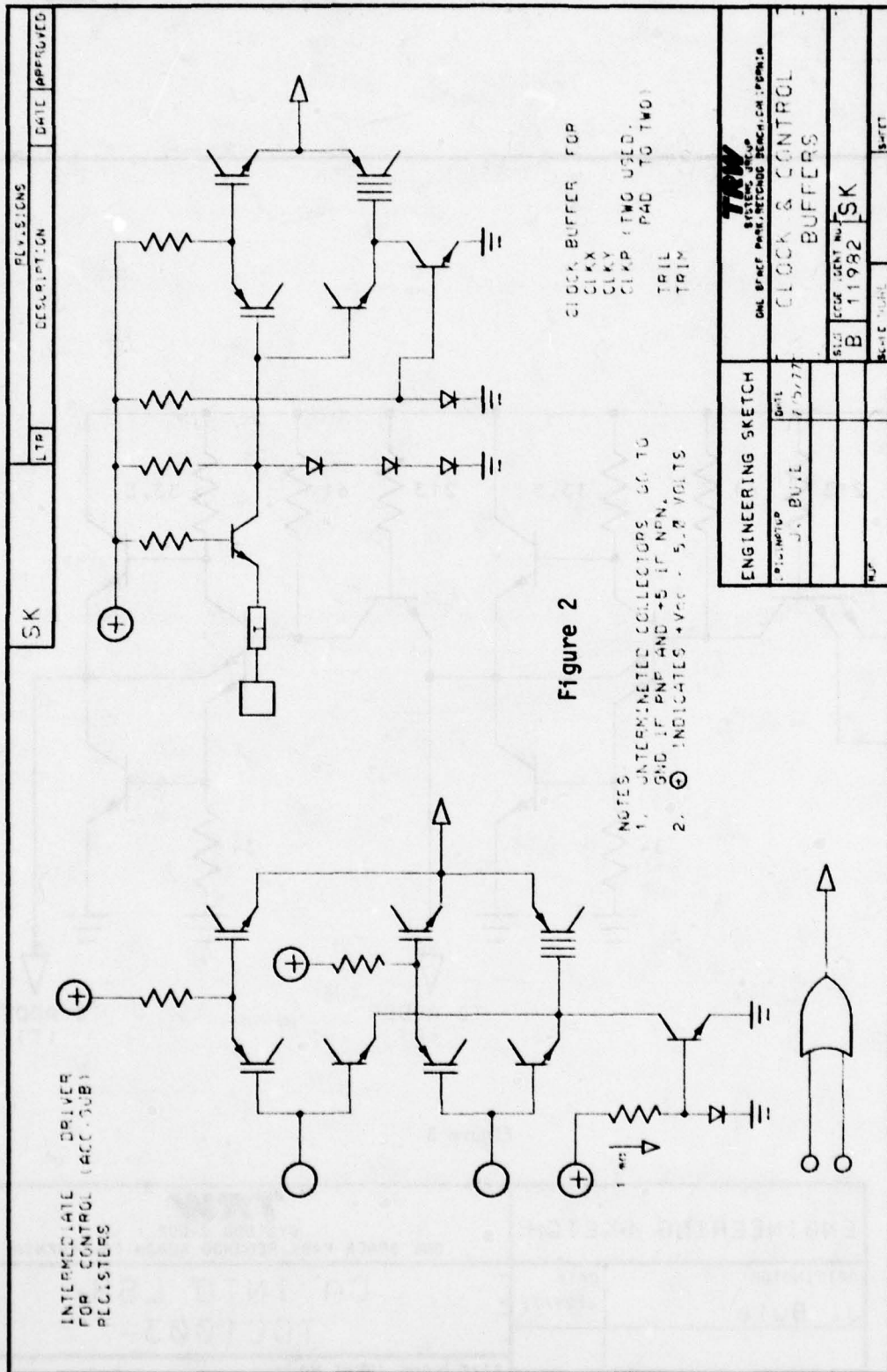


Figure 1

NOTE. UNTERMINATED COLLECTEDS GO TO
1. +5 IF NPN AND GND IF PNP

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							SHEET: 1	



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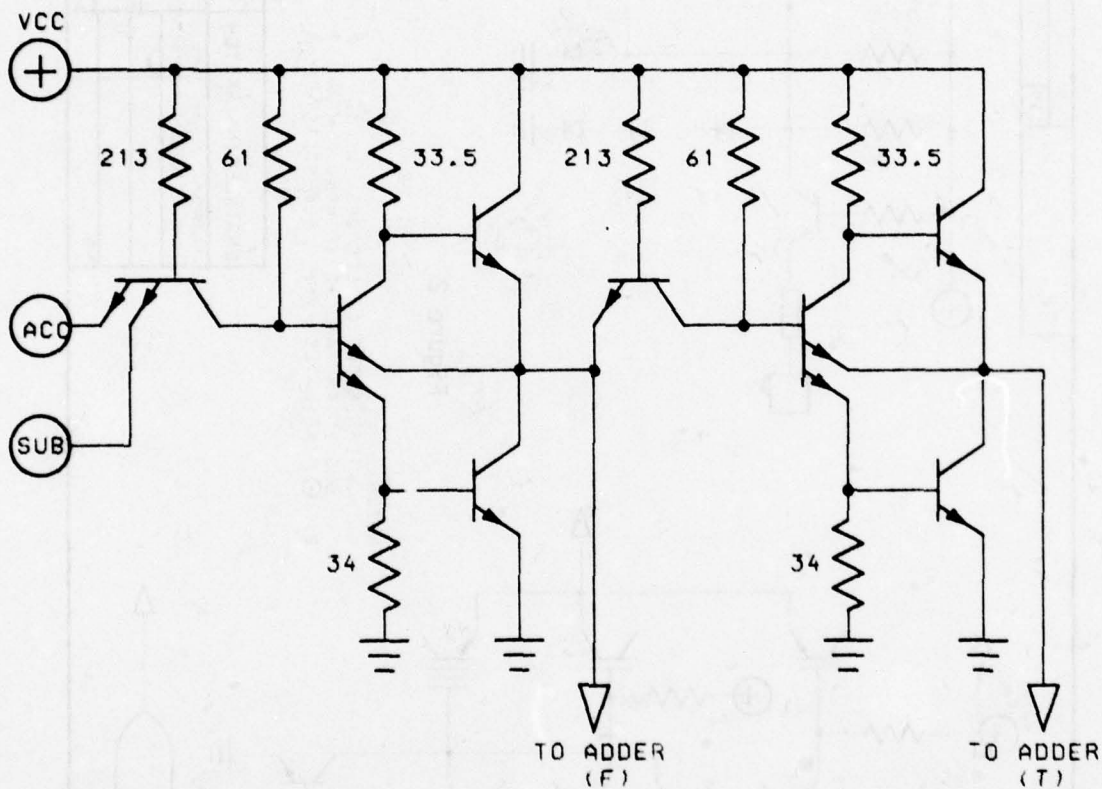
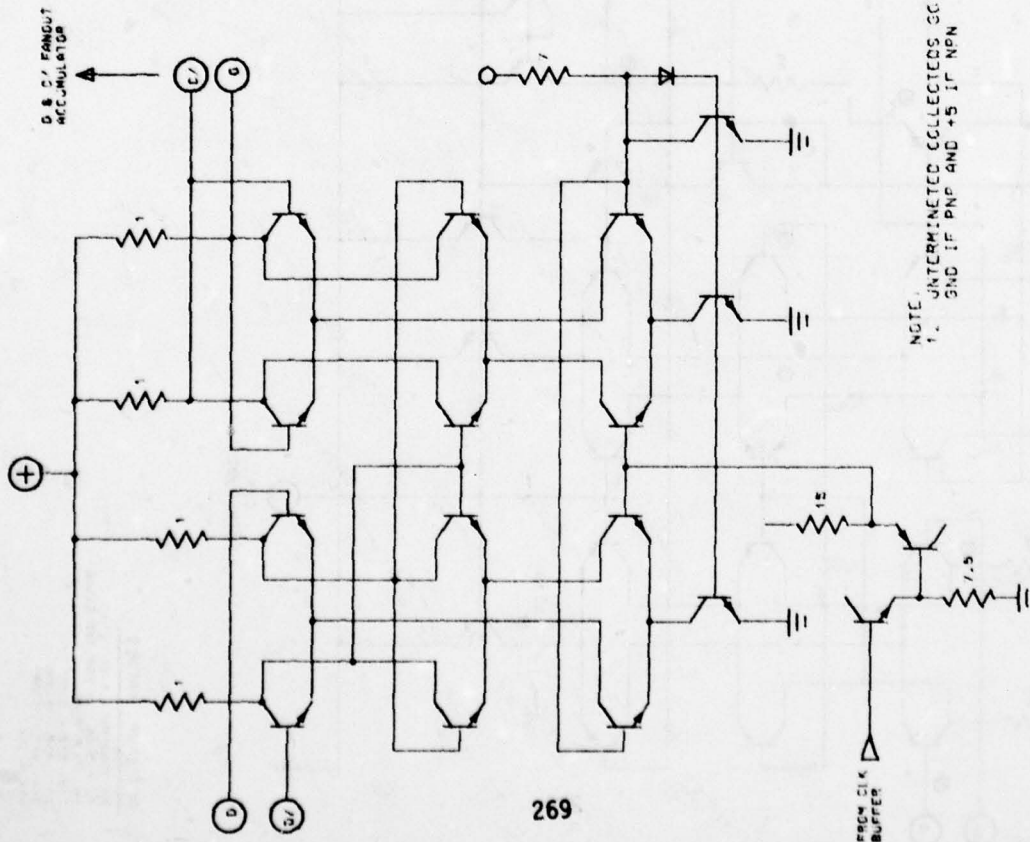


Figure 3

ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK, REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	CA INTO LSB TDC1003	
J. Bule	6/29/77		
		SIZE	CODE IDENT NO.
		A	11982
HJO		SK	
SCALE NONE		SHEET	

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NOTE: UNTERMINATED COLLECTORS GO TO
1. GND IF PNP AND +5 IF NPN

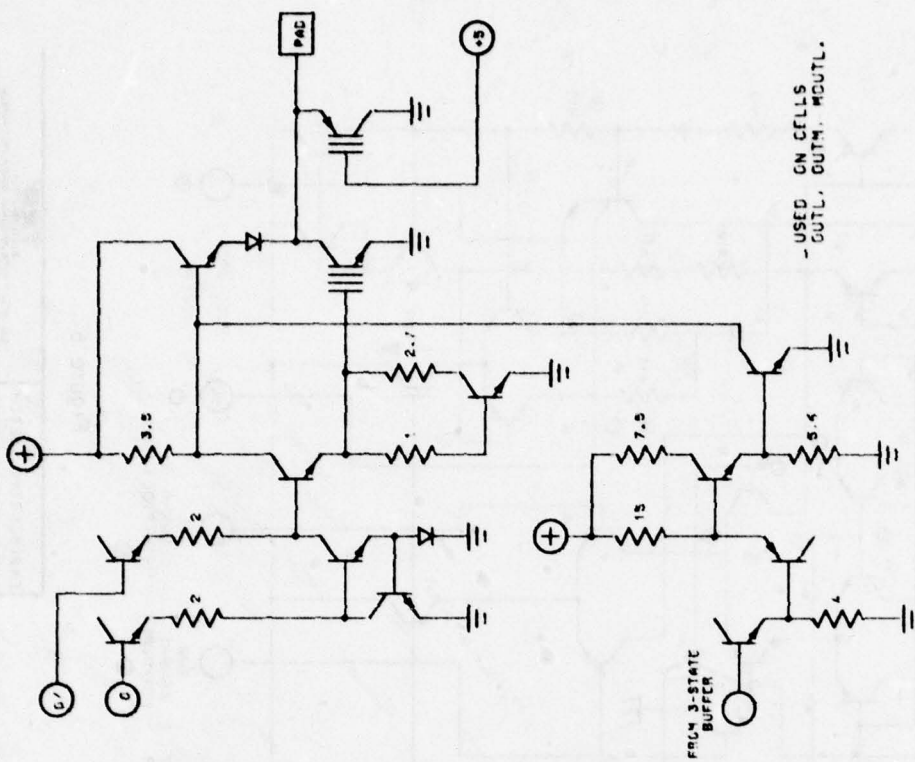


Figure 4

ENGINEERING SKETCH		ONE SPACE PAPER (SEE INSTRUCTIONS)	
DATE: 1/17/77	BY: J. BULE	PROJECT: TDC1003, 3 - STATE	REVISION: 1
		TITLE: OUTPUT REGISTER & BUFFER	
		SIZE: 11x17	SCALE: 1:1
		DATE: 11/82	SK
		NAME: NUNE	DESIGN

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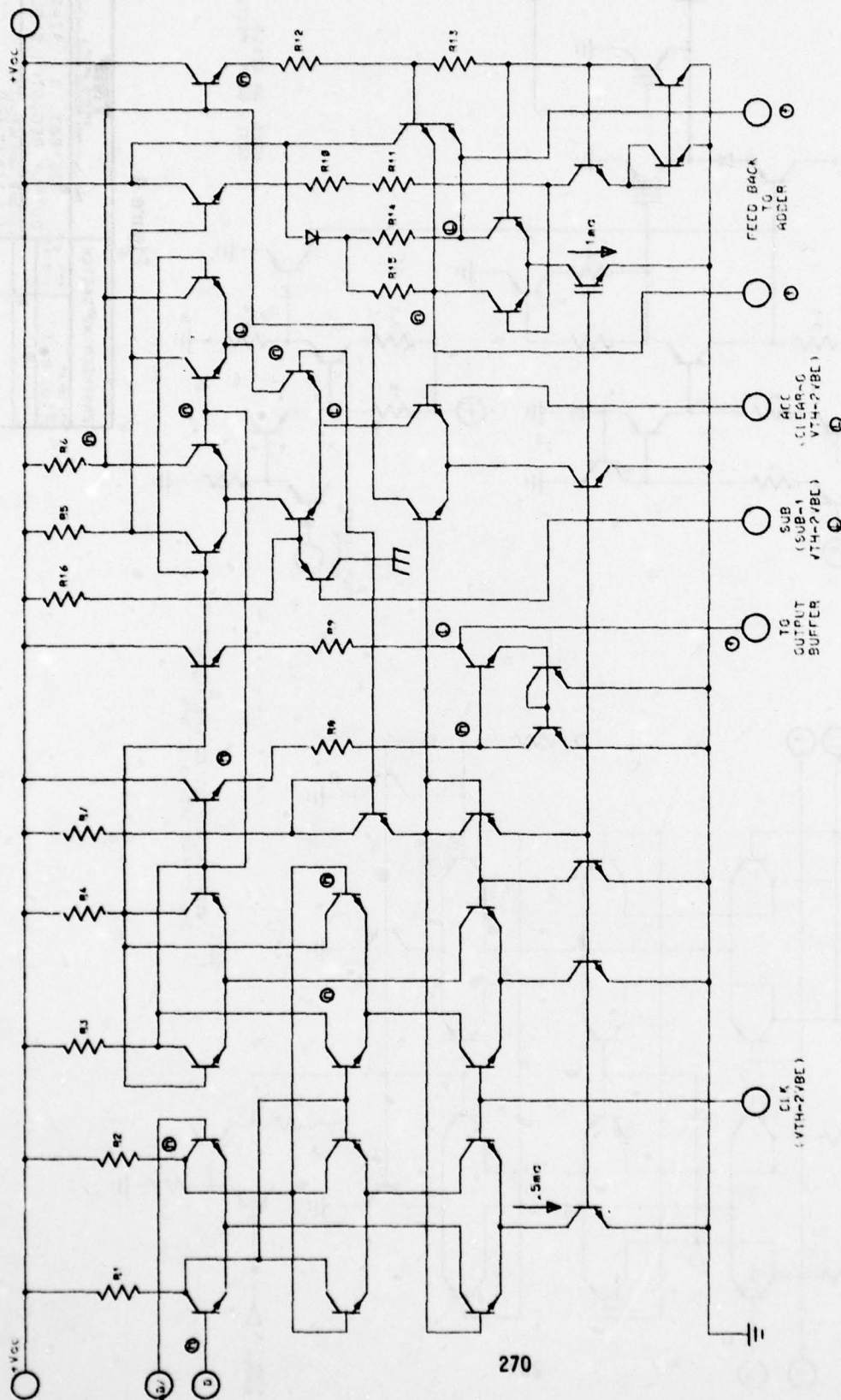


Figure 5

ENGINEERING SKETCH		DATE		BY	
DESIGNED	J. BULE	DATE	7/9/77	CHKD	W. J. HARRIS
PROJECT		TITLE		REV	
		C 11982		SK	

RESISTOR VALUES

R1 THRU R6 = 1.8K
R7 = 5.1K 7% FOR TNG CIRCUIT
R8, R9 = 2.2K
R10, R12 = 3.3K
R11, R13 = 8.2K
R14 = 5.1K
R15 = 15K

APPENDIX E

SPECIFICATION FOR SIGNAL PROCESSING DELAY LINE

INTRODUCTION

The signal processing delay line, SPDL, 3D current mode logic (CML) LSI is TTL compatible at inputs and outputs. The SPDL functionally provides the capability for parallel iterative FFT processor address sequencing in a pipelined mode. Each SPDL is composed of two shift register sections, shown in Figure 1. The upper section is used for upper address sequencing and the lower section is used for lower address sequencing relative to the FFT butterfly algorithm. The addresses of data points are input as time multiplexed upper and lower addresses at the A input and bit reversed time multiplexed upper and lower addresses at the B input. The upper and lower addresses are steered to their respective shift register sections by appropriately clocking the corresponding shift register. The upper point addresses are clocked by ACLF into the upper shift register, designated by subscript u in Figure 1; and the lower point addresses are clocked by BCLF into the lower shift register designated by subscript L in Figure 1. The upper output multiplexer selects addresses $n-4$ and $n-2$, where n is the address being generated and stored into SPDL from SPAC. The lower output multiplexer selects addresses $n-4$ and n .

1.0 FUNCTIONAL

The SPDL is composed of two shift register sections each containing two multiplexers and a five-bit shift register. The inputs are time multiplexed on A, B, or selected independently using the INSEL control from A or B. The tristate A and B outputs may be tied together for a common address destination by using complementary OUTAEN and OUTBEN signals or used independently.

The output multiplexer in each section provides selection from a tap or output from the end of the shift register.

1.1 The Input Multiplexer

Input addresses are shifted from TTL up to CML levels at the A and B inputs. Each input drives two-bit slices of the SPDL. The input requirement is listed in Table 1. The input multiplexer TTL control line INSEL drives twelve-bit slices. The input requirement is listed in Table 1.

TABLE 1. INPUT CHARACTERISTICS

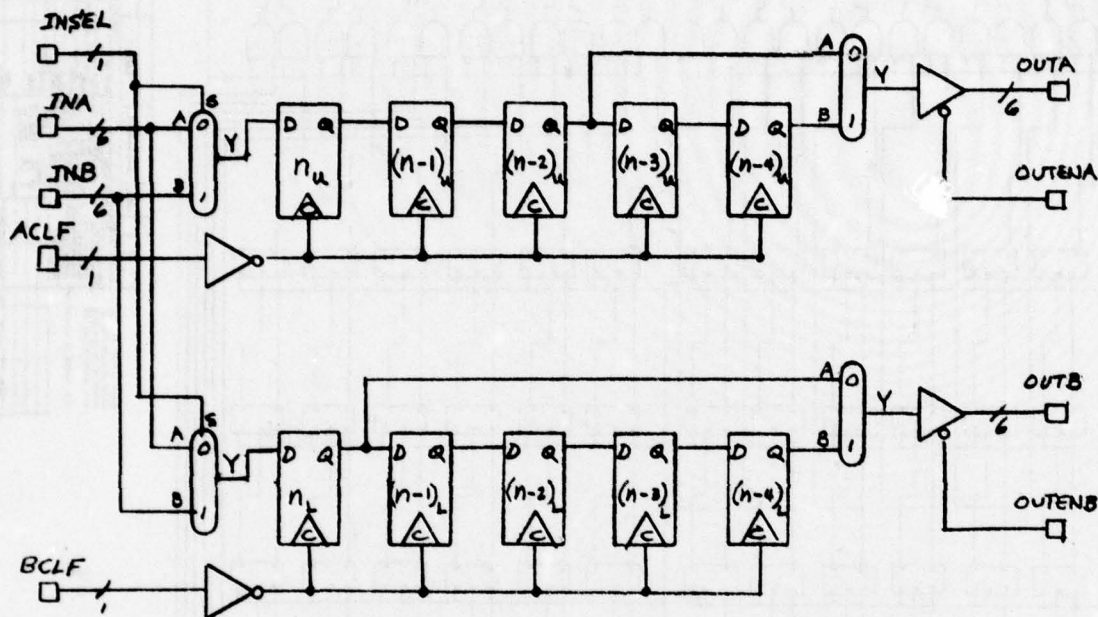
SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
INA or INB	Low Level Input Voltage	V_{ILD}		0.4	0.8	Volts
	High Level Input Voltage	V_{IHD}	2.0	3.4		Volts
	Low Level Input Current $V_{ILD} = .3$ volts	I_{ILD}		-.500	-.700	mA
	High Level Input Current $V_{IHD} = 3.4$ volts	I_{IHD}		50	70	μ A
	Setup Time Data Stable to Clock	T_{SUD}	20			ns
INSEL	Low Level Input Voltage	V_{ILC}		0.4	0.8	Volts
	High Level Input Voltage	V_{IHC}	2.0	3.4		
	Low Level Input Current $V_{ILD} = .3$ volts	I_{ILC}		-7.0	-9.0	mA
	High Level Input Current $V_{IHD} = 3.4$ V	I_{IHC}		70	90	μ A
	Setup Time Control Stable to clock	T_{SUC}	30			ns

SIGNAL	LOGIC	FUNCTION
INA or INB	0	False Address
	1	True Address
INSEL	0	Select A Input (INA)
	1	Select B Input (INB)

SK

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
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Signal Processing Delay Line 3D LSI

ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA	
ORIGINATOR	DATE	Figure 1 SPDL Block Diagram	
<i>A. Hudson</i>	9/30/75		
SIZE	CODE IDENT NO.	SK	
A	11982		
SCALE		273	SHEET 1 OF

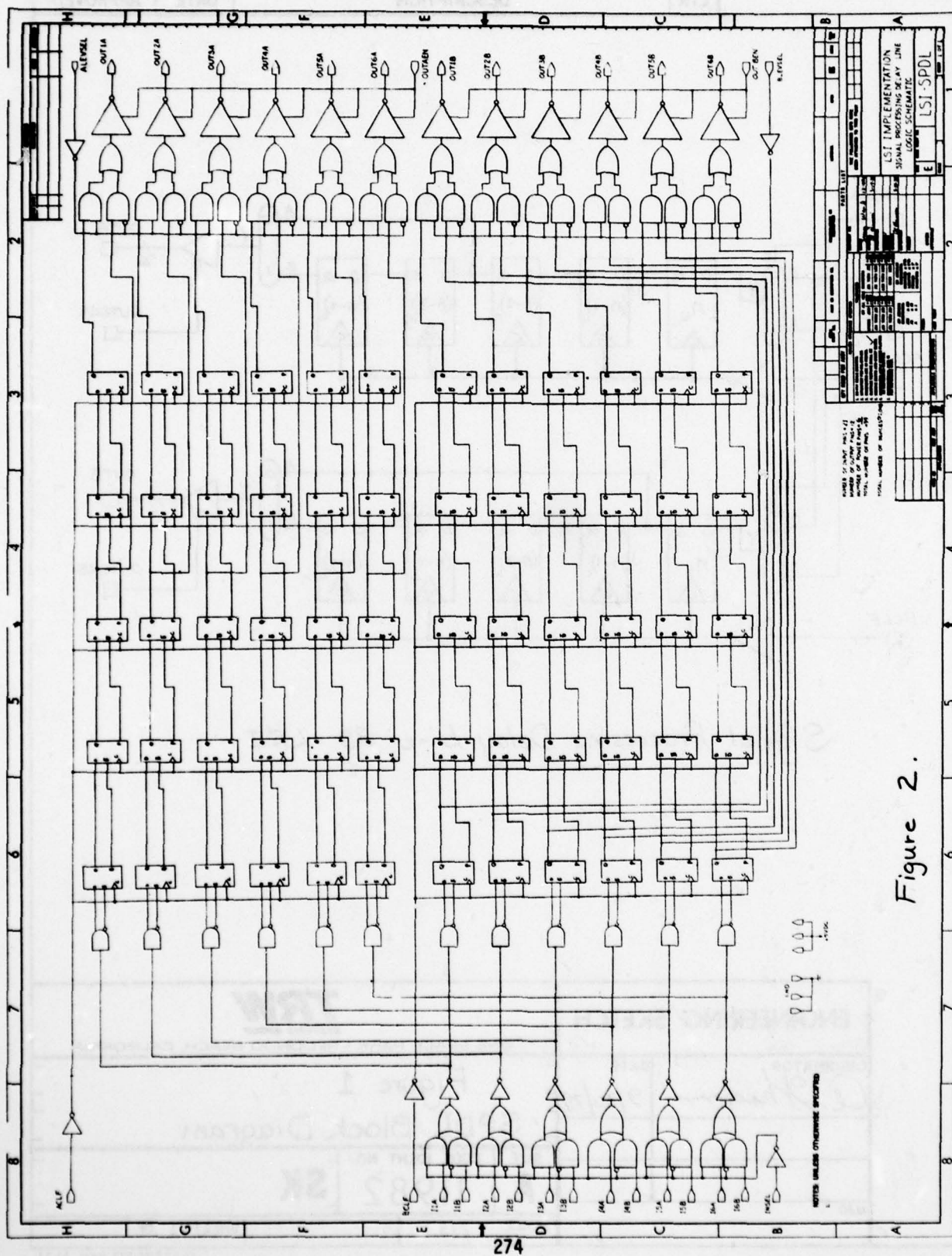


Figure 2.

1.2 The Shift Registers

There are twelve five-bit CML shift registers in the SPDL, one shift register per bit slice. Each slice has its own dedicated clock driver driving its shift register. The input specification for the clock load, driving six clock drivers is listed in Table 2. The shift register advances on the negative going edge clock at the input of the SPDL. Each shift register section is clocked by an independent input clock. The characteristics of the CML registers used in the shift register is given in Table 2.

1.3 The Output Multiplexers

Each of the two CML shift register sections is tapped differently to provide access at different delays. These taps are selected using the output multiplexers in each section. The tap selections are listed in Table 3 along with the multiplexer to output characteristics.

1.4 Output Tristate Drivers

The output drivers are enabled to a tristate bus by applying a low input at the OUTEN lines. A high input selects the outputs at a section off. The characteristics of the output drivers are listed in Table 4.

2.0 CHARACTERISTIC OPERATING RATINGS

The SPDL operates over the margins listed in Table 5.

TABLE 2. SHIFT REGISTER CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
ACLF or BCLF	Low Level Input Voltage	V_{ILP}		0.4	0.8	V
	High Level Input Voltage	V_{IHP}	2.0	3.4		V
	Low Level Input Current	I_{ILP}		-3.5	-4.5	mA
	High Level Input Current	I_{IHP}		40	50	μ A
	Propagation Time Clock into Flip-Flop	T_{PDLHP}		15	25	ns
	Clock Asymmetry V_{IUP} at 10 MHz	V_{ILSM}		50	60	%
CML D F/F Q1-Q5	Propagation Time Q output from clock (H or L)	T_{PDQC}		7	10	ns
	Clock Frequency	f_c		10	16	MHz
	Application Clock Frequency	f_{AC}		4	6	MHz

TABLE 3. OUTPUT MULTIPLEXER CHARACTERISTICS

SIGNAL	STATE	REGISTER TAP
ALEVSEL	0	$(n-2)u$
	1	$(n-4)u$
BLEVSEL	0	n_L
	1	$(n-4)L$

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
ALEVSEL BLEVSEL	High Level Input Voltage	V_{IH}	2.0	3.4		Volts
	Low Level Input Voltage	V_{IL}		.4	.8	Volts
	High Level Input Current	I_{IH}		40	50	
	Low Level Input Current	I_{IL}		-3.5	-4.5	mA
	Propagation Time select output law	T_{pds}		15	22	ns

TABLE 4. OUTPUT DRIVER CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
OUT(1-6)A or OUT(1-6)B	Output High Voltage	V_{OHD}	2.4	3.5		V
	Output Low Voltage	V_{OLD}		0.4	0.6	V
	Output High Current $V_{OH} = 2.4V$	I_{OHD}		-200	-1000	μA
	Output High Current $V_{OL} = 0.4V$	I_{OLD}	6			mA
	Propagation Time Multiplexer input to Driver Output (High to low) ON 50 pf 800 Ω	T_{POHL}		22	30	ns
	Propagation Time Multiplexer input to Driver Output (Low to high) ON 50 pf 800 Ω	T_{PNLH}		30	45	ns
	Propagation Time Driver input select to driver output (OFF to LOW = $V_{CC} \rightarrow V_{OLD}$) 50 pf 800 Ω	T_{PONHL}		40	60	ns

SIGNAL	LOGIC	FUNCTION
OUTAEN or	0	Select output ON
OUTBEN	1	Select output OFF

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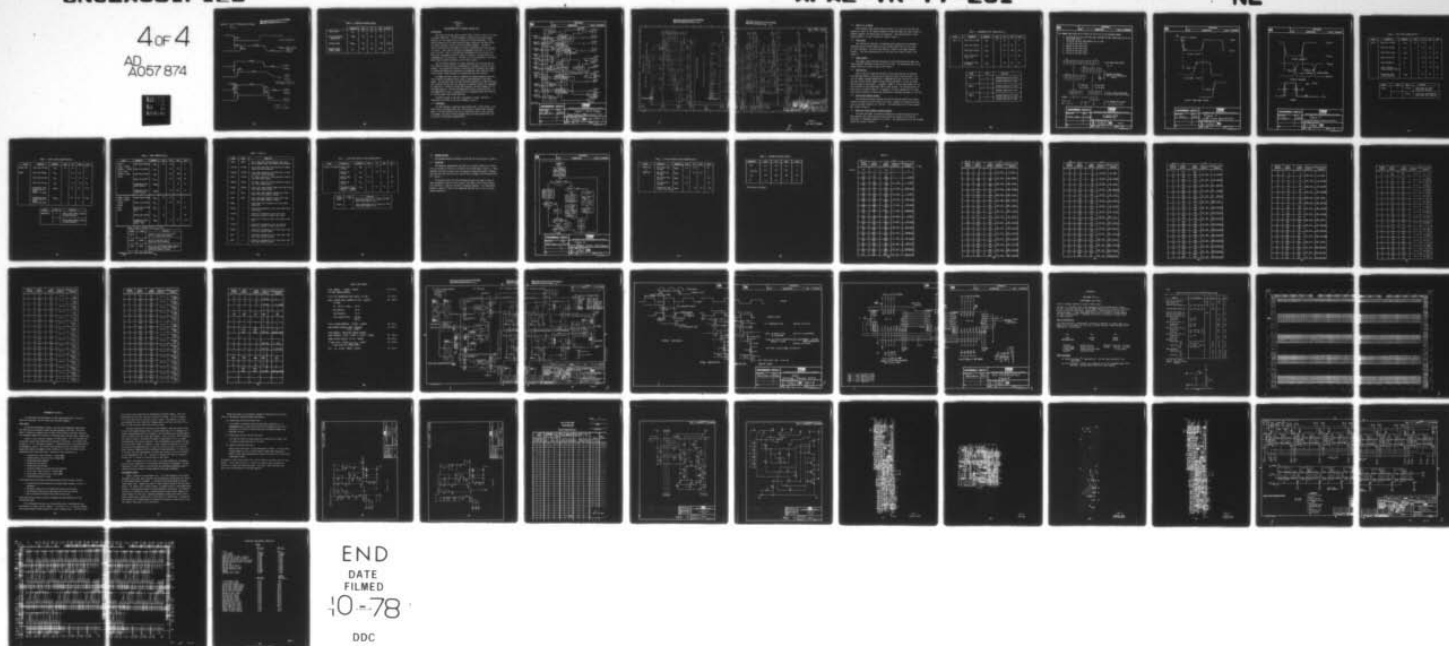
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OUTPUT MUX & TRISTATE DRIVER

FIG. 3

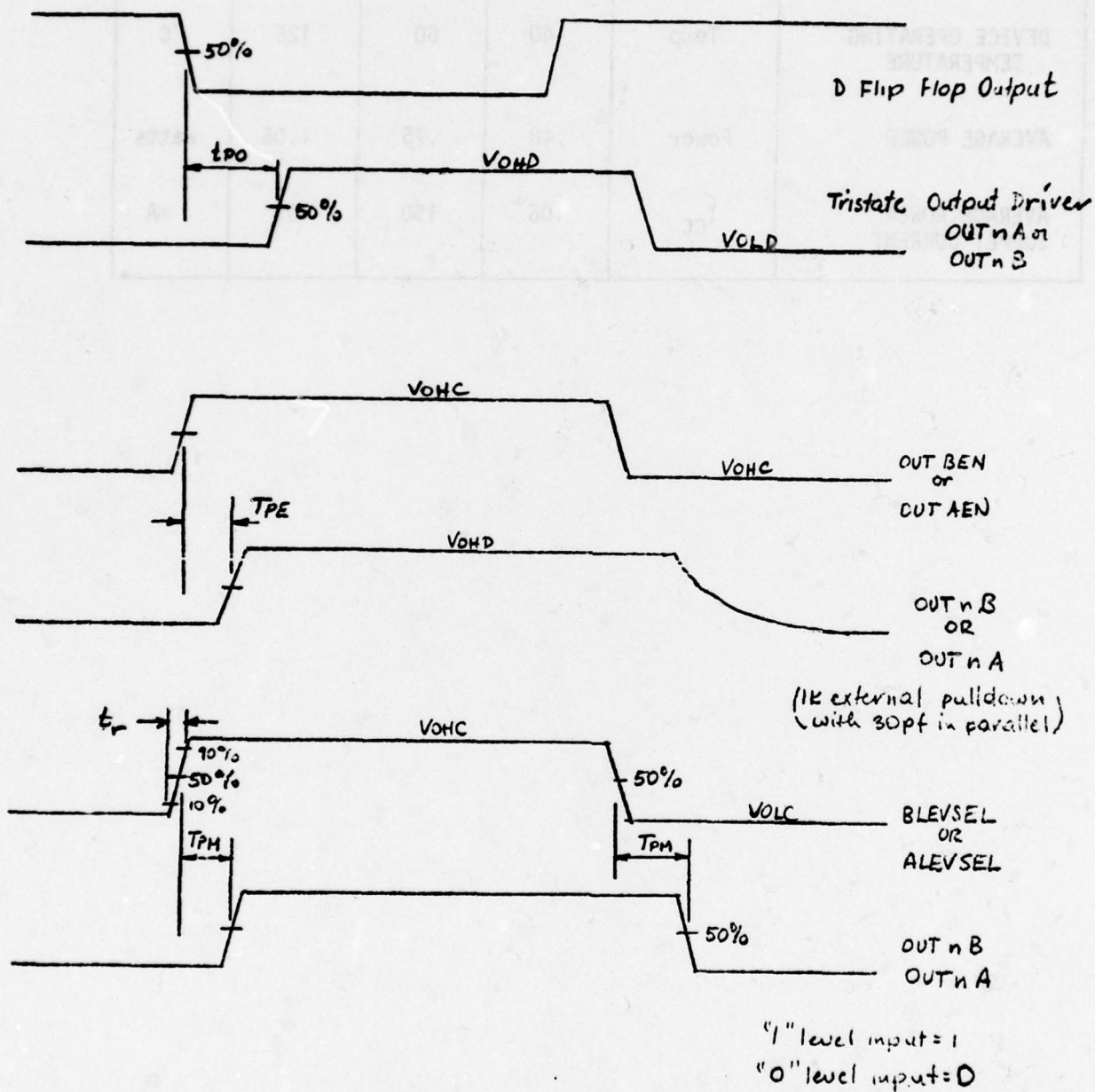


TABLE 5. ABSOLUTE MAXIMUM RATINGS

	PARAMETER	MIN	TYP	MAX	UNITS
POWER SUPPLY	V_{CC}	4.5	5.0	5.5	V
DEVICE OPERATING TEMPERATURE	Temp	-40	60	125	°C
AVERAGE POWER	Power	.48	.75	1.05	watts
AVERAGE POWER SUPPLY CURRENT	I_{CC}	105	150	190	mA

APPENDIX F

SPAC 1

SPECIFICATION FOR FFT ADDRESS CONTROL CHIP

INTRODUCTION

The signal processing address control (SPAC) 3D CML-EFL chip is TTL input and output compatible. The SPAC generates, on start preset, three address sequences for time domain parallel iterative FFT kernel processors. These address sequences are the upper butterfly address sequence, the lower butterfly address sequence, and the coefficient address sequence. The SPAC or SPAC's are dynamically programmable to accept a converted $\log_2 N$ code for FFT's of N points. SPAC's may be cascaded to accommodate extensions, E , of 2^{E+1} points per SPAC. That is, one SPAC will accommodate 32 points and $E=0$, two SPAC's will accommodate 1024 points and $E=1$ extension, and three SPAC's will accommodate up to 32,768 points. The SPAC LSI set also generates a last level signal used to orderly terminate each FFT kernel process.

The coefficient addresses are always generated left justified with the first thetas (θ) equal to 0 or π independent of the number of points (N) programmed. The progressive increased θ resolution with increasing level number is accomplished using carry injection to succeeding lower significant coefficient counter stages by means of a propagating ones shift register.

The upper and lower butterfly addresses are always generated right justified selecting incremental points across a spread dependent on the level number. The resultant upper and lower butterfly addresses are time multiplexed and transmitted to both real and imaginary FFT memories directly for sequential FFT operation or indirectly through SPDL sequencer and then to memory for FFT pipelined operation. The SPAC has detectors for end of spread and level. It uses combinatorial logic in conjunction with a propagating ones shift register to flag the proper level-spread operation.

The block diagram of the SPAC is presented in Figure 1 and this is interpreted in 3D logic in the logic schematic, Figure 2.

1.0 FUNCTIONAL

The SPAC receives a converted $\log_2 N$ program code, a start preset, a free running clock, an output select line, and carries-in linking other cascaded SPAC's. The SPAC transmits five bits of coefficient address (left justified to the MSB), five bits of time multiplexed upper and lower address bits, and carries-out linking other cascaded SPAC's.

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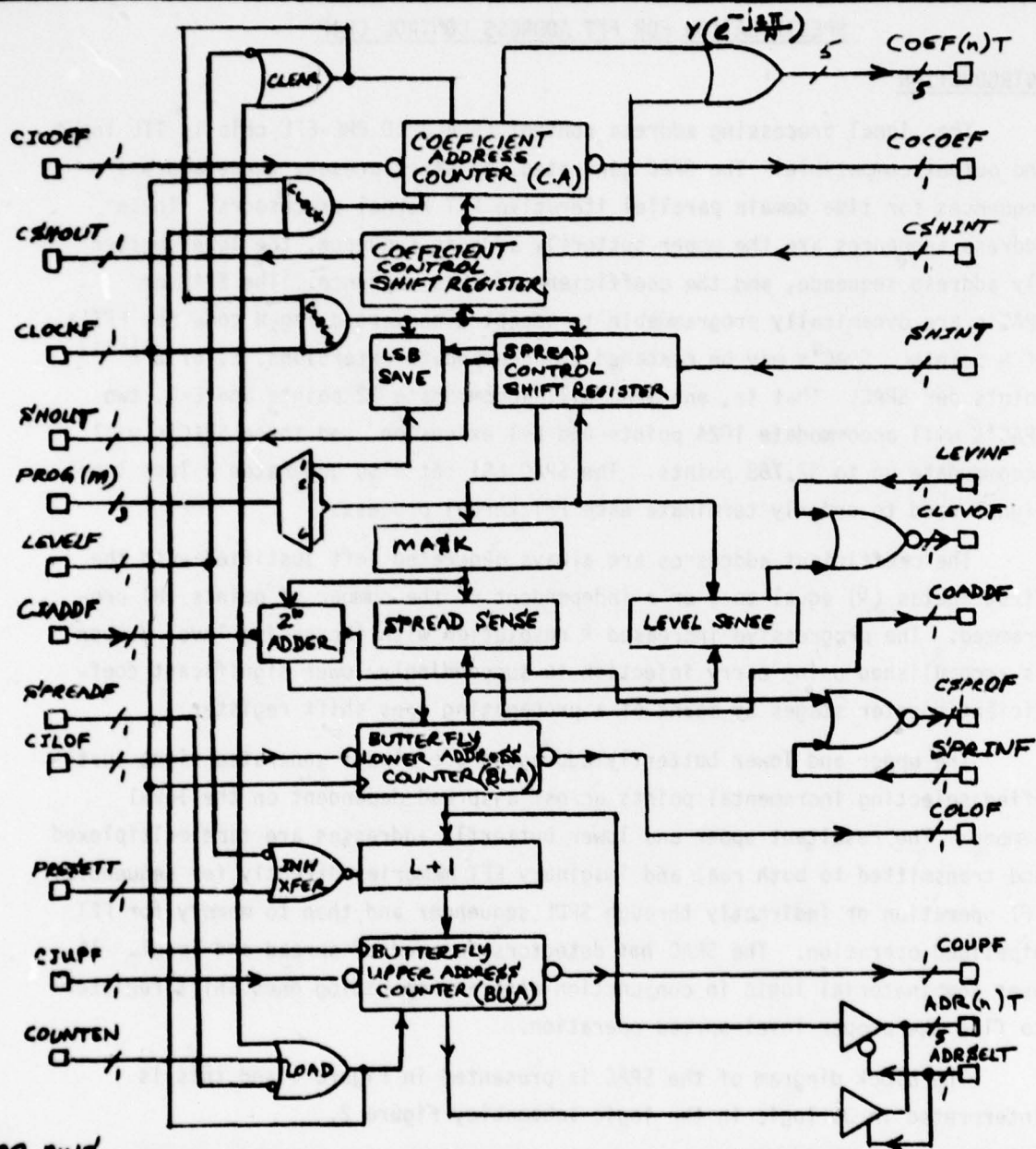
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Figure 1, Block Diagram
Signal Processing Address Control LSI

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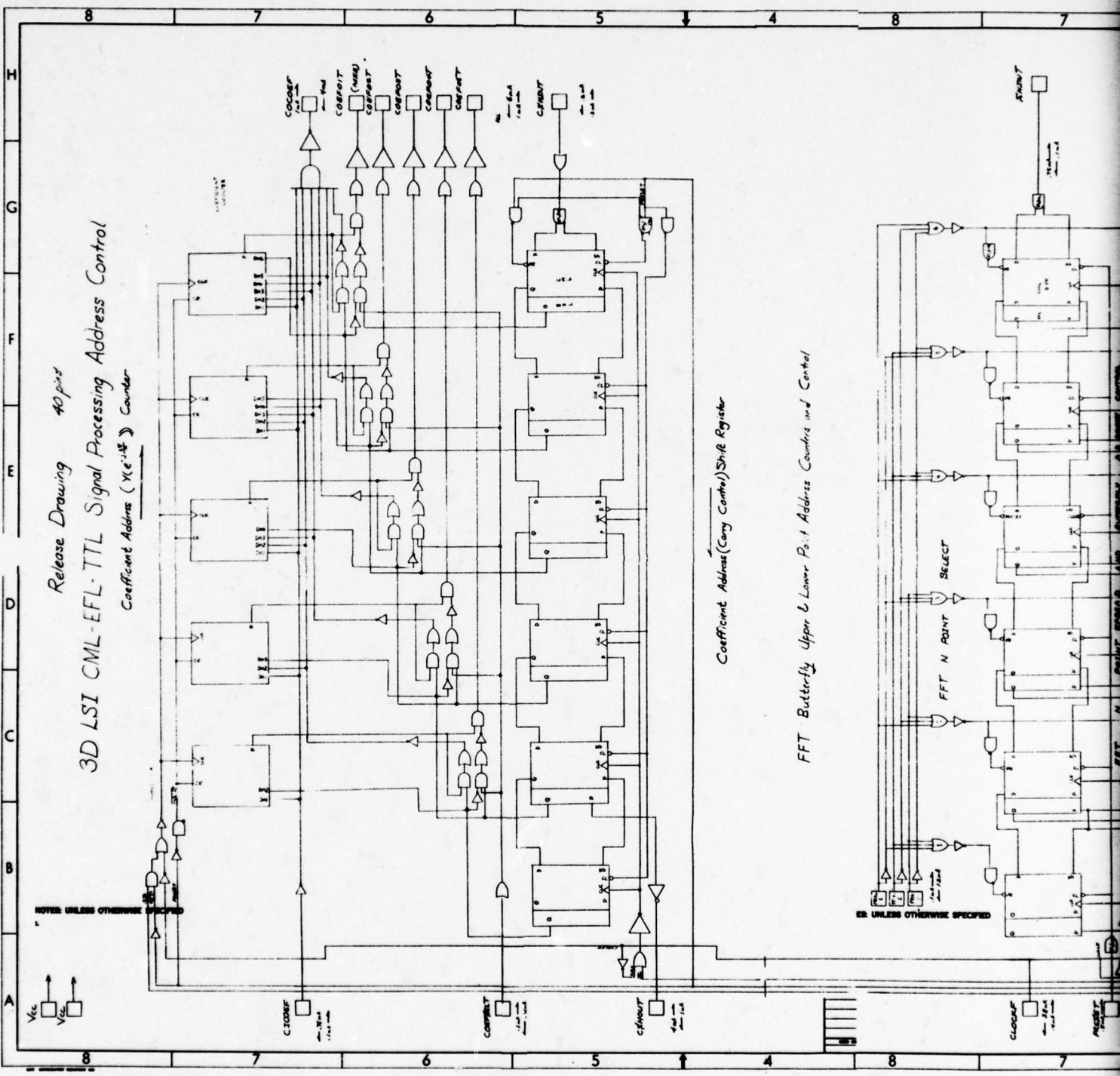
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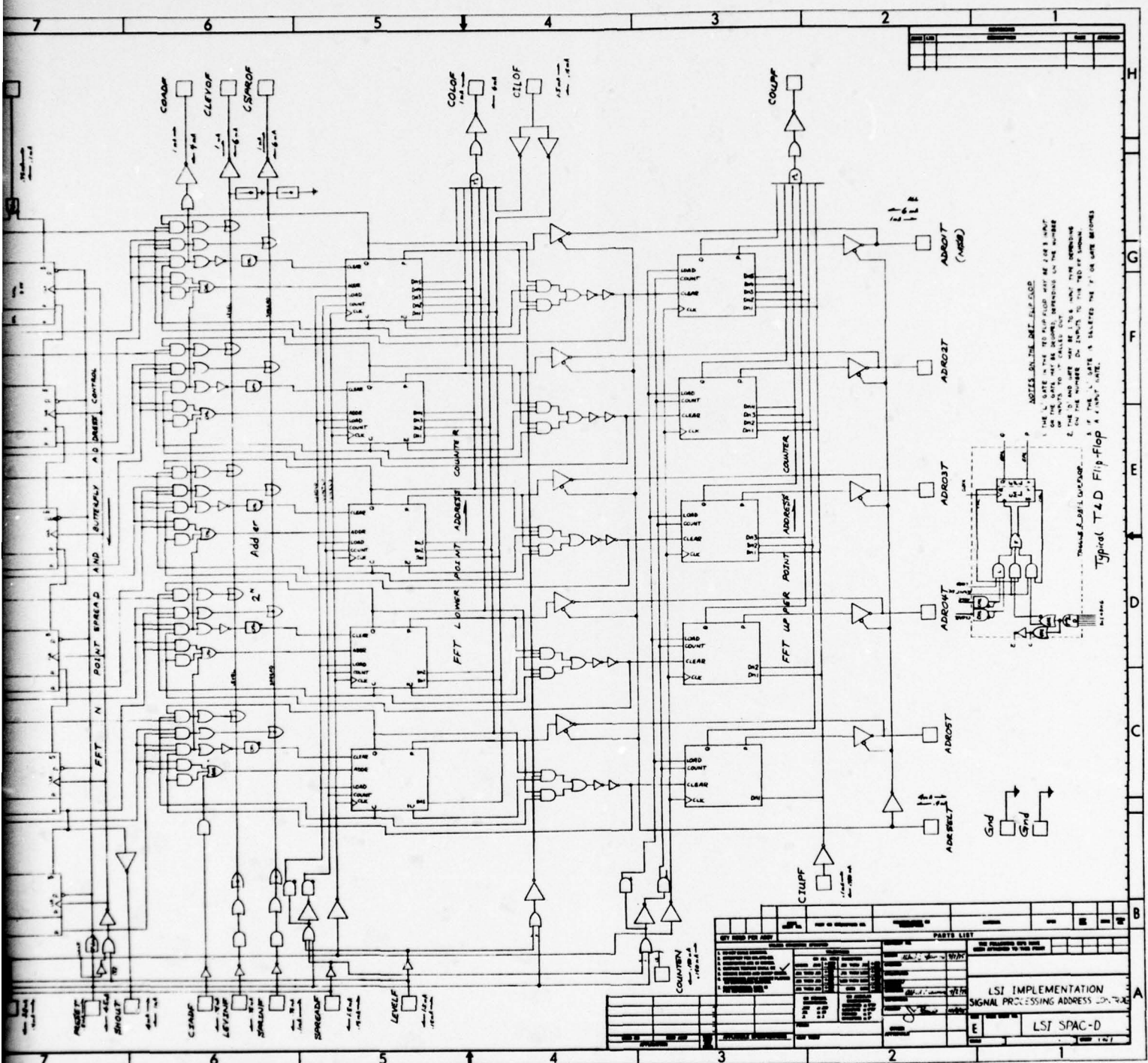


Figure 2
SPAC LOGIC DIAGRAM

1.1 PROG 1, 2, 3 Inputs

The converted $\log_2 N$ code defined in Figure 3 is input into the SPAC and decoded to select an $\frac{N}{2}$ address sequence for both the upper and lower butterfly address counters, and $\log_2 N$ levels of execution. The characteristics of the $\log_2 N$ PROG 1, 2, and 3 inputs are listed in Table 1.

1.2 Clock Input

The clocking of registers is performed using internally and externally generated controls which enable the free running input clock to count load, or shift registers. The clock distribution is shown in the logic diagram, Figure 2. The input characteristics of the clock are listed in Table 2 and Figure 4.

1.3 Output Select

The output select provides the means of time multiplexing the upper and lower butterfly addresses on one set of five lines. The characteristics of the output select are listed in Table 3 and Figure 5.

1.4 SPAC Carries

Each of the five registers/counters in one given SPAC may be cascaded into adjoining SPAC's, using the carry input and output lines provided. The rate of address sequence generation is dependent upon the rippling of carries from the initial counter stage, through intervening SPAC's, to the last SPAC and the input to the counter. In general, there is a pair delay added into the carry cascade for each additional SPAC in the cascade. The characteristics of each carry is listed in Table 4. In general, all carry outputs use TTL totem pole drivers capable of sinking the equivalent of low power Schottky TTL (LS-TTL).

1.5 Coefficient Address Outputs

The coefficient address outputs are derived from the coefficient address counter and output using TTL totem pole drivers, capable of sinking the equivalent of low power Schottky TTL, (LS-TTL). The characteristics of these outputs are listed in Table 5.

1.6 Upper and Lower Butterfly Address Outputs

The upper and lower FFT butterfly addresses are time multiplexed on the SPAC address lines using tristate drivers which are capable of sinking the equivalent of low power Schottky TTL (LS-TTL). The characteristics of the tristate driver are listed in Table 6.

TABLE 1. PROGRAMMING INPUT CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
PROG 1,2,3	Input High Voltage	V_{IHP}	2.0	3.4		V
	Input Low Voltage	V_{ILP}		0.4	0.8	V
	Input High Current	I_{IHP}		50	100	μA
	Input Low Current ($V_{ILP} = .4V$)	I_{ILP}		-9	-1.2	mA
	Propagation Time to Preset	T_{PDP}		20	30	ns

SIGNAL	LOGIC	FUNCTION
PROG 1	0	Decoded $\log_2 N$ bit 2^2 false
	1	Decoded $\log_2 N$ bit 2^2 true
PROG 2	0	Decoded $\log_2 N$ bit 2^1 false
	1	Decoded $\log_2 N$ bit 2^1 true
PROG 3	0	Decoded $\log_2 N$ bit 2^0 false
	1	Decoded $\log_2 N$ bit 2^0 true

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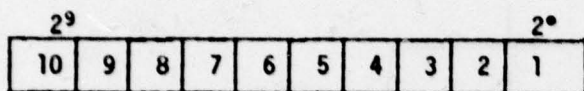
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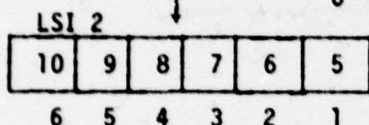
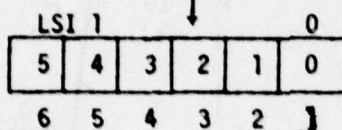
THE PROGRAM CODE ENTERS THE FFT POINT SIZE (N) AS N/2 IN THE FOLLOWING FORMAT.

- 0 ALL BITS IN THE 5-BIT SLICE ARE ZERO, INCLUDING THE MOST SIGNIFICANT BIT OF THE LOWER ORDER SLICE.
- 1 THE MSB OF THE NEXT LOWER ORDER SLICE IS A ONE.
- 2 1ST BIT OF THE 5-BIT SLICE
- 3 2ND BIT OF THE 5-BIT SLICE
- 4 3RD BIT OF THE 5-BIT SLICE
- 5 4TH BIT OF THE 5-BIT SLICE
- 6 5TH BIT OF THE 5-BIT SLICE



10 BIT WORD SIGNIFYING $\frac{N}{2}$

$$\frac{N}{2} = 2^n$$

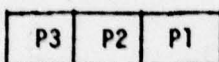
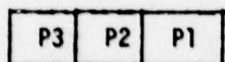


BREAKING THE WORD UP INTO 2 6-BIT OVERLAPPING FIELDS

LSB ZERO

BIT POSITION
ON IN OCTAL

BIT POSITION
ON IN OCTAL



THESE 2 FIELDS ARE RECODED IN THE LSI INTO 6-BIT FIELDS.

EXAMPLE: IF $\frac{N}{2} = 2^9 = 10000 / 00000$

1024 PT FFT

$N/2 = 512 = 2^9$

1 0 0 0 0 0
6 6

0 0 0 0 0 0
0

THE PROGRAM CODE BECOMES:

6₈, 0₈ for 2 LSI's

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LSI ADDRESS CONTROL
PROGRAMMING CODE

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Figure 3

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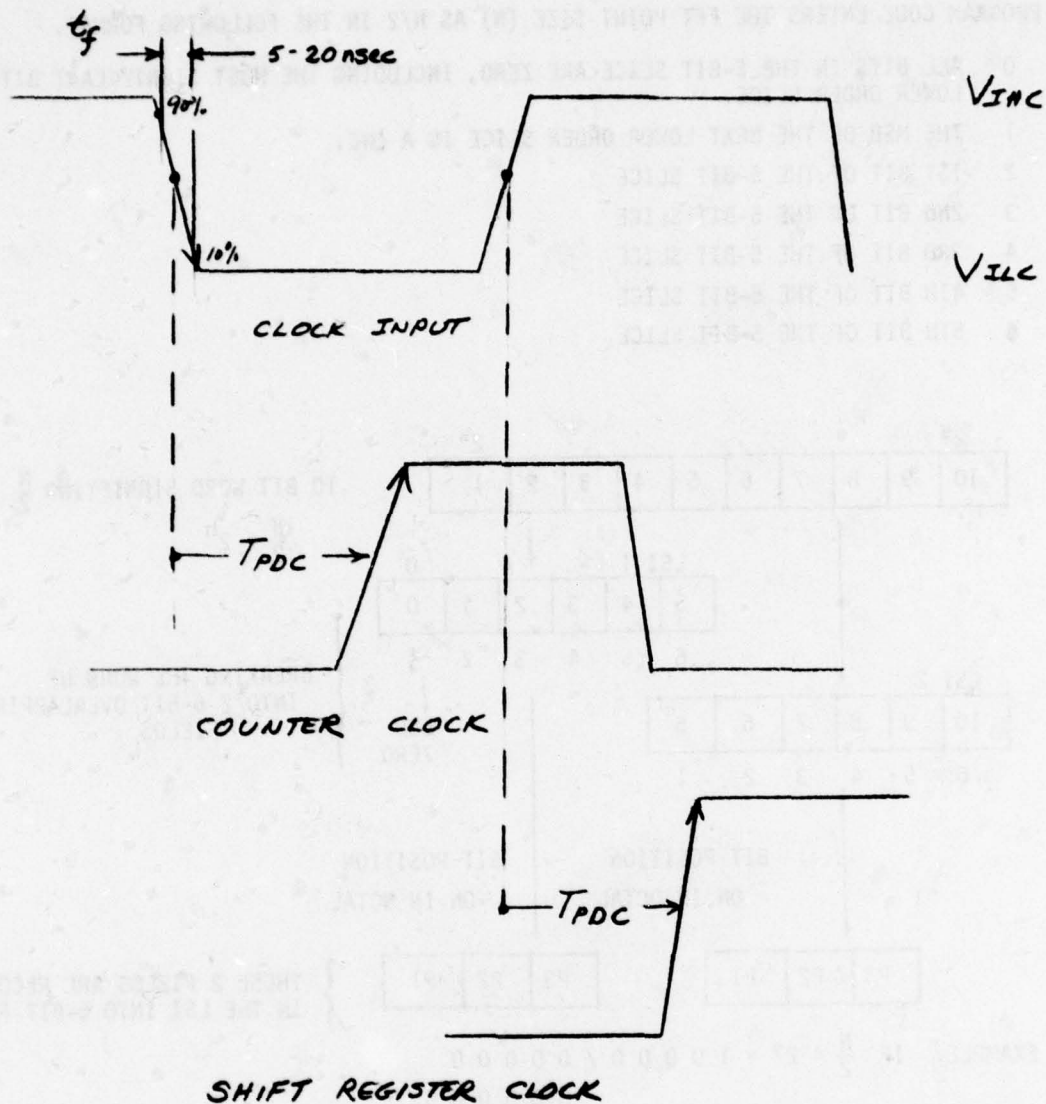
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Figure 4
SPAC Clock Specification

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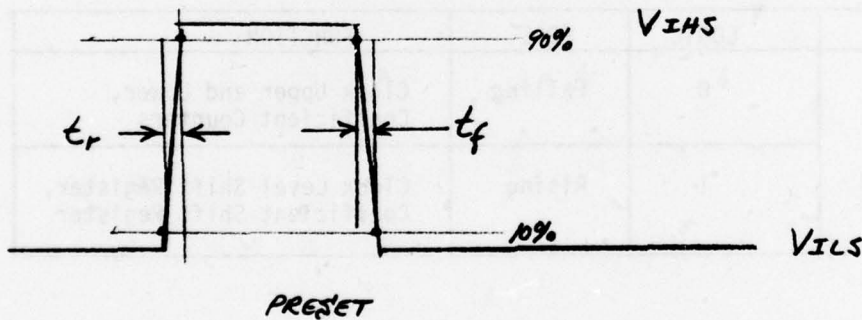
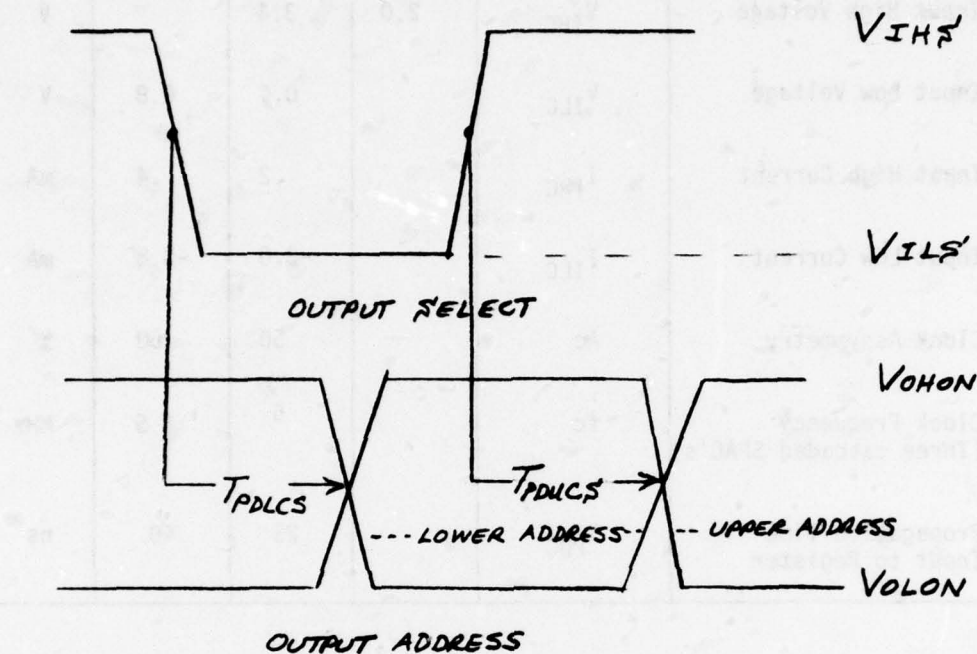
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Figure 5
Output Select Characteristics

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TABLE 2. INPUT CLOCK CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
CLOCK F	Input High Voltage	V_{IHC}	2.0	3.4		V
	Input Low Voltage	V_{ILC}		0.4	0.8	V
	Input High Current	I_{IHC}		.2	.4	mA
	Input Low Current	I_{ILC}		-3.0	-3.8	mA
	Clock Assymetry	Ac		50	60	%
	Clock Frequency (Three cascaded SPAC's)	fc		5	< 5	MHz
	Propagation Time Input to Register	T_{PDC}		25	40	ns

SIGNAL	LOGIC	EDGE	FUNCTION
CLOCK F	0	Falling	Clock Upper and Lower, Coefficient Counters
	1	Rising	Clock Level Shift Register, Coefficient Shift Register

TABLE 3. OUTPUT SELECT CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
ADRSEL MCT6	Input High Voltage	V_{IHS}	2.0	3.4		V
PRESET	Input Low Voltage	V_{ILS}		0.4	0.8	V
	Input High Current	I_{IHS}		0.3	0.5	mA
	Input Low Current	I_{ILS}		-3.0	-4.5	mA
	Propagation Time, (Lower Counter to Output) (50 pf 1K load)	T_{PDLCS}		25	40	nsec
	Propagation Time, (Upper Counter to Output) (50 pf 25K load)	T_{PDUCS}		35	50	nsec

SIGNAL	LOGIC	FUNCTION
ADRSELMCT6	0	Select Lower Address Counter to Output Address
	1	Select Upper Address Counter to Output Address

TABLE 4. CARRY CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONIC	MIN	TYP	MAX	UNIT
CICOEF, SHINT, LEVINF, CSPRINF, CIADDF, CILOF, CIUPF SPREADF, CSHINT LEVELF	Input High Voltage	V_{IHR}	2.0	3.4		V
	Input Low Voltage	V_{ILR}		0.4	0.8	V
	Input High Current	V_{IHR}		50*	100*	μA
	Input Low Current	I_{ILR}		-.5*	-.75*	mA
	Propagation Time, Input Inverter	T_{PDRHL}		7	10	ns
	Propagation Time, Input Inverter	$T_{PDR LH}$		15	20	ns
CSHOUT, COCOEF, SHOUT, CLEVOF* CSPROF COADDF COLOF COUPF	Output High Voltage	V_{OHR}	2.4	3.5		V
	Output Low Voltage	V_{OLR}		0.4	0.6	V
	Output High Current $V_{OHR} = 2.4V$	I_{OHR}	-1			mA
	Output Low Current	I_{OLR}	4*			mA
	Propagation Time, Output Driver 20 pf 4K	T_{PDRO}		15	20	nsec

*COLOF, CLEVOE, & CSPROF require $I_{OLR} = 6 \text{ mA}$

SIGNAL	LOGIC	FUNCTION
CSHINT	1	Identify of Most Significant SPAC for $\theta = \pi$ Coefficient Address
CSHINT	CSHOUT	Carry In from Carry Out of Coefficient Shift Register
CICOEF	COCOEF	Carry Into Coefficient Address Counter from Carry Out of lower order SPAC Coefficient Address Counter

*SPREADF & LEVEL F INPUT LOADS ARE DOUBLED
CILOF

TABLE 4 (cont'd)

SIGNAL	LOGIC	FUNCTION
SHINT	SHOUF	Carry Into Level Shift Register from Carry Out of higher order SPAC level shift register.
CLEVINF	CLEVOF	Carry Into Level Bus from Carry Out of lower order SPAC level detector.
CSPRINF	CSPROTF	Carry Into Spread Bus from Carry Out of lower order SPAC Spread Detector.
LEVELF	CLEVOF	All SPAC's receive as inputs the most significant SPAC level output.
SPREADF	CSPROF	All SPAC's receive as inputs the most significant SPAC spread output.
CIADDF	COADDF	Carry Into Lower Counter Adder from lower order SPAC lower counter adder.
CILOF	COLOF	Carry Into Lower Address Counter from lower order SPAC Lower Address Counter.
CIUPF	COUPF	Carry Into Upper Address Counter from lower order SPAC Upper Address Counter.
SHOUT	1	Coefficient shift register out from higher order SPAC.
COCOEF	0	Cumulative propagating carry from lower order coefficient.
CLEVOTF	0	Cumulative propagating carry from level detection cascade in lower order SPAC's.
SHOUT	0	Level shift register output from higher order SPAC
CSPROTF	0	Cumulative propagating carry from spread detection cascade in lower order SPAC's.
COADDF	0	Cumulative propagating carry from lower order SPAC lower counter adder.
COLOF	0	Cumulative propagating carry from lower order SPAC lower address counter.
COUPF	0	Cumulative propagating carry from lower order SPAC upper address counter.

TABLE 5. COEFFICIENT ADDRESS OUTPUT/CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONICS	MIN	TYP	MAX	UNIT
COEF01T to COEF05T	Output High Voltage	V_{OHF}	2.4	3.5		V
	Output Low Voltage	V_{OLF}		0.4	0.6	V
	Output High Current	I_{OHF}	-1.0			mA
	Output Low Current	I_{OLF}	6.0			mA
	Propagation Time Register to Output *(50 pf, 2.5K Ω)	T_{PDF}		45	60	ns

SIGNAL	LOGIC	FUNCTION
COEF01	1	Most significant bit of θ angle for SPAC coefficient address slice.
COEF05	1	Least significant bit of θ angle for SPAC coefficient address slice.

2.0 MAXIMUM RATINGS

The maximum operating ratings for the SPAC 3D LSI are given in Table 7.

3.0 OPERATION

The addresses generated by the SPAC for a parallel iterative 512 point FFT are included in Table 8, as derived from the flow chart, Figure 6. These addresses are used to access real and imaginary data points and/or intermediate data and sine and cosine FFT coefficients as shown in the representative FFT, Figure 7.

The maximum control and data propagation times are shown in Table 9. These propagation times are also shown in the SPAC critical timing diagram (Fig. 8) which is used for two SPAC's connected together. The interconnect diagram is shown in Figure 9 for expanding the SPAC from a 5-bit to 10-bit address generation.

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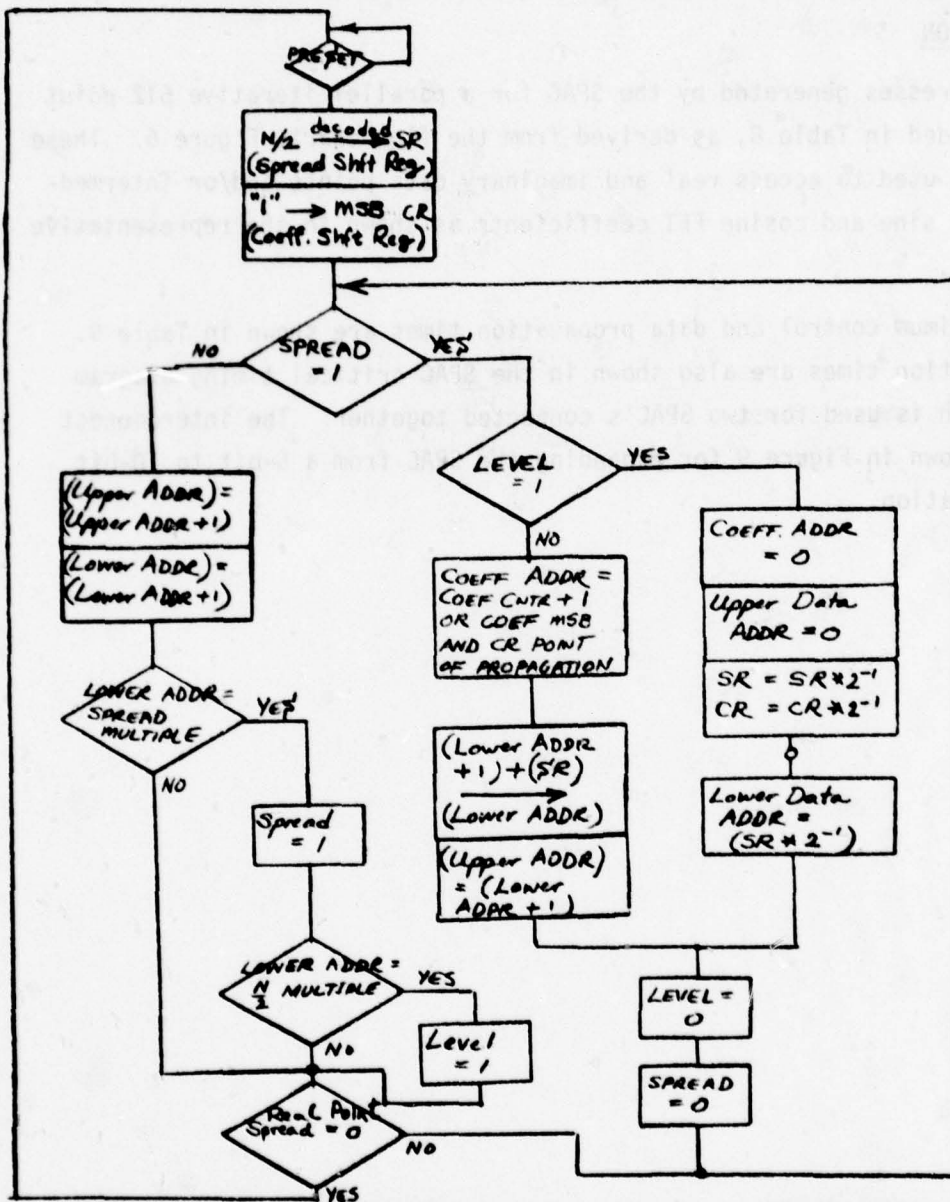
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Figure 6

FFT Address Control Flow Diagram

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TABLE 6. TRISTATE ADDRESS DRIVER CHARACTERISTICS

SIGNAL	PARAMETER	MNEMONICS	MIN	TYP	MAX	UNIT
ADRO1- ϕ TT7 to ADRO5- ϕ TT7	ON, Output High Voltage	V _{OHON}	2.4	3.5		VV
	ON, Output Low Voltage	V _{OLON}		0.4	0.6	V
	ON, Output High Current	I _{OHON}	-1.0			mA
	ON, Output Low Current	I _{OLON}	6.0			mA
	Propagation Time (50 pf 2.5K load)*	T _{PDON}		35	50	nsec

TABLE 7. MAXIMUM OPERATING RATINGS

PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	4.5	5.0	5.5	V
T_{junction}	-4.0	+25	+125	°C
I_{CC}^*	210	300	380	mA
P^*	1.2	1.5	1.7	W

*Preliminary Estimates

TABLE 8

Preset

(Sp. C.)	U	L	L.C.	COEFFICIENT ADDRESS
SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	
512	0	512	1	0
512 ↓ 1023	0 ↓ 511	512 ↓ 1023	1	0 (0°)
256 ↓ 511	0 ↓ 255	256 ↓ 511	2 (2)	0 (0°)
256 ↓ 511	512 ↓ 767	768 ↓ 1023	3 (2)	128 ($\pi/2$)
128 ↓ 255	0 ↓ 127	128 ↓ 255	4 (3)	0 (0°)
128 ↓ 255	256 ↓ 383	384 ↓ 511	5 (3)	128 ($\pi/2$)
128 ↓ 255	512 ↓ 639	640 ↓ 767	6 (3)	64 ($\pi/4$)
128 ↓ 255	768 ↓ 895	896 ↓ 1023	7 (3)	192 ($3\pi/4$)
64 ↓ 127	0 ↓ 63	64 ↓ 127	8 (4)	0 (0°)
64 ↓ 127	128 ↓ 191	192 ↓ 255	9 (4)	64 ($\pi/4$)
64 ↓ 127	256 ↓ 319	320 ↓ 383	10 (4)	128 ($\pi/2$)
64 ↓ 127	384 ↓ 447	448 ↓ 511	11 (4)	192 ($3\pi/4$)
64 ↓ 127	512 ↓ 575	576 ↓ 639	12 (4)	32 ($\pi/8$)
64 ↓ 127	640 ↓ 703	704 ↓ 764	13 (4)	96 ($3\pi/8$)
64 ↓ 127	768 ↓ 831	832 ↓ 895	14 (4)	160 ($5\pi/8$)
64 ↓ 127	896 ↓ 959	960 ↓ 1023	15 (4)	224 ($7\pi/8$)

$\pi = 256$

Sp. C	U	L	L.C.	
SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level COUNTER	COEFFICIENT ADDRESS
32	0	32		
63	31	63	16 (5)	0 (0°)
32	64	96		
63	95	127	17 (5)	32 ($\pi/8$)
32	128	160		
63	159	191	18 (5)	64 ($\pi/4$)
32	192	224		
63	223	255	19 (5)	96 ($3\pi/8$)
32	256	288		
63	287	319	20 (5)	128 ($\pi/2$)
32	320	352		
63	351	383	21 (5)	160 ($5\pi/8$)
32	384	416		
63	415	447	22 (5)	192 ($3\pi/4$)
32	448	480		
63	479	511	23 (5)	224 ($7\pi/8$)
32	512	544		
63	543	575	24 (5)	16 ($\pi/16$)
32	576	608		
63	607	639	25 (5)	48 ($3\pi/16$)
32	640	672		
63	671	703	26 (5)	80 ($5\pi/16$)
32	704	736		
63	735	767	27 (5)	126 ($7\pi/16$)
32	768	800		
63	799	831	28 (5)	144 ($9\pi/16$)
32	832	864		
63	863	895	29 (5)	176 ($11\pi/16$)
32	896	928		
63	927	959	30 (5)	208 ($13\pi/16$)
32	960	992		
63	991	1023	31 (5)	240 ($15\pi/16$)

Sp.C	U	L	L.C.	
SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
16	0	16		
31	15	31	32 (6)	0 (0°)
16	32	48		
31	47	63	33 (6)	16 ($\pi/16$)
16	64	80		
31	79	95	34 (6)	32 ($\pi/8$)
16	96	112		
31	111	127	35 (6)	48 ($3\pi/16$)
16	128	144		
31	143	159	36 (6)	64 ($\pi/4$)
16	160	176		
31	175	191	37 (6)	80 ($5\pi/16$)
16	192	208		
31	207	223	38 (6)	96 ($3\pi/8$)
16	224	240		
31	239	255	39 (6)	112 ($7\pi/16$)
16	256	272		
31	271	287	40 (6)	128 ($\pi/2$)
16	288	304		
31	303	319	41 (6)	144 ($9\pi/16$)
16	320	336		
31	335	351	42 (6)	160 ($5\pi/8$)
16	352	368		
31	367	383	43 (6)	176 ($11\pi/16$)
16	384	400		
31	399	415	44 (6)	192 ($3\pi/4$)
16	416	432		
31	431	447	45 (6)	208 ($13\pi/16$)
16	448	464		
31	463	479	46 (6)	224 ($7\pi/8$)
16	480	466		
31	495	511	47 (6)	240 ($15\pi/16$)

Sp.C	U	L	L.C.	
SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
16	512	528		
31	527	543	48 (6)	8 ($\pi/32$)
16	544	560		
31	559	575	49 (6)	24 ($3\pi/32$)
16	576	592		
31	591	607	50 (6)	40 ($5\pi/32$)
16	608	624		
31	623	639	51 (6)	56 ($7\pi/32$)
16	640	656		
31	655	671	52 (6)	72 ($9\pi/32$)
16	672	688		
31	687	703	53 (6)	88 ($11\pi/32$)
16	704	720		
31	719	735	54 (6)	104 ($13\pi/32$)
16	736	752		
31	751	767	55 (6)	120 ($15\pi/32$)
16	768	784		
31	783	799	56 (6)	136 ($17\pi/32$)
16	800	816		
31	815	831	57 (6)	152 ($19\pi/32$)
16	832	848		
31	847	863	58 (6)	168 ($21\pi/32$)
16	864	880		
31	879	895	59 (6)	184 ($23\pi/32$)
16	896	912		
31	911	927	60 (6)	200 ($25\pi/32$)
16	928	944		
31	943	959	61 (6)	216 ($27\pi/32$)
16	960	976		
31	975	991	62 (6)	232 ($29\pi/32$)
16	992	1008		
31	1007	1023	63 (6)	248 ($31\pi/32$)

SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL(Level) COUNTER	COEFFICIENT ADDRESS
8	0	8		
15	7	15	64 (7)	0 (0°)
8	16	24		
15	23	31	65 (7)	8 ($\pi/32$)
8	32	40		
15	39	47	66 (7)	16 ($\pi/16$)
8	48	56		
15	55	63	67 (7)	24 ($3\pi/32$)
8	64	72		
15	71	79	68 (7)	32 ($\pi/8$)
8	80	88		
15	87	95	69 (7)	40 ($5\pi/32$)
8	96	104		
15	103	111	70 (7)	48 ($3\pi/16$)
8	112	120		
15	119	127	71 (7)	56 ($7\pi/32$)
8	128	136		
15	135	143	72 (7)	64 ($\pi/4$)
8	144	152		
15	151	159	73 (7)	72 ($9\pi/32$)
8	160	168		
15	167	175	74 (7)	80 ($5\pi/16$)
8	176	184		
15	183	191	75 (7)	88 ($11\pi/32$)
8	192	200		
15	199	207	76 (7)	96 ($3\pi/8$)
8	208	216		
15	215	223	77 (7)	104 ($13\pi/32$)
8	224	232		
15	231	239	78 (7)	112 ($7\pi/16$)
8	240	248		
15	247	255	79 (7)	120 ($15\pi/32$)

SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
8 15	256 263	264 271	80 (7)	128 ($\pi/2$)
8 15	272 279	280 287	81 (7)	136 ($\frac{17\pi}{32}$)
8 15	288 295	296 303	82 (7)	144 ($\frac{9\pi}{16}$)
8 15	304 311	312 319	83 (7)	152 ($\frac{19\pi}{32}$)
8 15	320 327	328 335	84 (7)	160 ($\frac{5\pi}{8}$)
8 15	336 343	344 351	85 (7)	168 ($\frac{21\pi}{32}$)
8 15	352 359	360 367	86 (7)	176 ($\frac{11\pi}{16}$)
8 15	368 375	376 383	87 (7)	184 ($\frac{23\pi}{32}$)
8 18	384 391	392 399	88 (7)	192 ($\frac{3\pi}{4}$)
8 15	400 407	408 415	89 (7)	200 ($\frac{25\pi}{32}$)
8 15	416 423	424 431	90 (7)	208 ($\frac{13\pi}{16}$)
8 15	432 439	440 447	91 (7)	216 ($\frac{27\pi}{32}$)
8 15	448 455	456 463	92 (7)	224 ($\frac{7\pi}{8}$)
8 15	464 471	472 479	93 (7)	232 ($\frac{29\pi}{32}$)
8 15	480 487	488 495	94 (7)	240 ($\frac{15\pi}{16}$)
8 15	496 503	504 511	95 (7)	248 ($\frac{31\pi}{32}$)

SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
8 15	512 519	520 527	96 (7)	4 $\left(\frac{\pi}{64}\right)$
8 15	528 535	536 543	97 (7)	12 $\left(\frac{3\pi}{64}\right)$
8 15	544 551	552 559	98 (7)	20 $\left(\frac{5\pi}{64}\right)$
8 15	560 567	568 575	99 (7)	28 $\left(\frac{7\pi}{64}\right)$
8 15	576 583	584 591	100 (7)	36 $\left(\frac{9\pi}{64}\right)$
8 15	592 599	600 607	101 (7)	44 $\left(\frac{11\pi}{64}\right)$
8 15	608 615	616 623	102 (7)	52 $\left(\frac{13\pi}{64}\right)$
8 15	624 631	632 639	103 (7)	60 $\left(\frac{15\pi}{64}\right)$
8 15	640 647	648 655	104 (7)	68 $\left(\frac{17\pi}{64}\right)$
8 15	656 663	664 671	105 (7)	76 $\left(\frac{19\pi}{64}\right)$
8 15	672 679	680 687	106 (7)	84 $\left(\frac{21\pi}{64}\right)$
8 15	688 695	696 703	107 (7)	92 $\left(\frac{23\pi}{64}\right)$
8 15	704 711	712 719	108 (7)	100 $\left(\frac{25\pi}{64}\right)$
8 15	720 727	728 735	109 (7)	108 $\left(\frac{27\pi}{64}\right)$
8 15	736 743	744 751	110 (7)	116 $\left(\frac{29\pi}{64}\right)$
8 15	752 759	760 767	111 (7)	124 $\left(\frac{31\pi}{64}\right)$

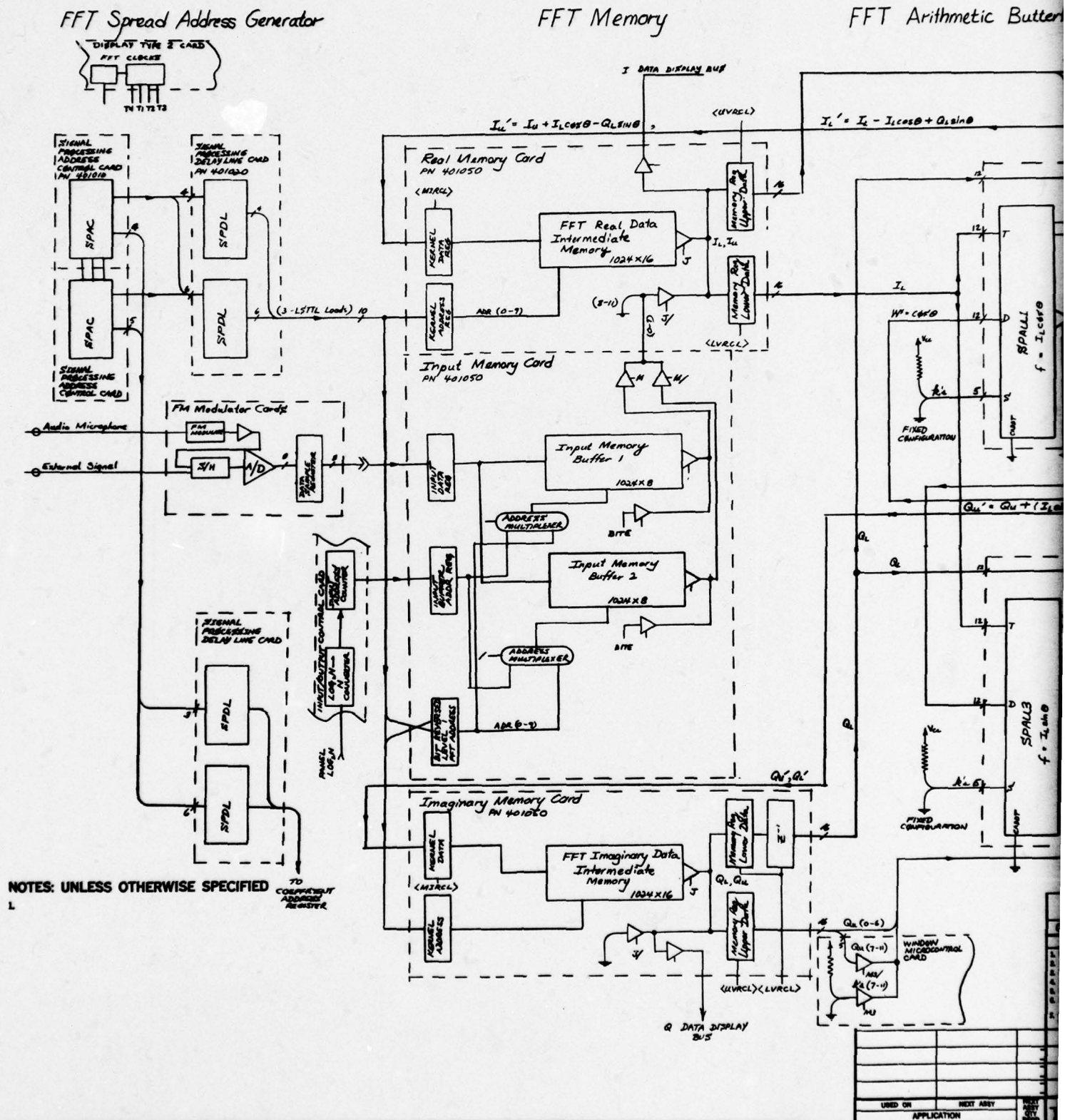
SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
8 15	768 775	776 783	112 (7)	132 $\left(\frac{33\pi}{64}\right)$
8 15	784 791	792 799	113 (7)	140 $\left(\frac{35\pi}{64}\right)$
8 15	800 807	808 815	114 (7)	148 $\left(\frac{37\pi}{64}\right)$
8 15	816 823	824 831	115 (7)	156 $\left(\frac{39\pi}{64}\right)$
8 15	832 839	840 847	116 (7)	164 $\left(\frac{41\pi}{64}\right)$
8 15	848 855	856 863	117 (7)	172 $\left(\frac{43\pi}{64}\right)$
8 15	864 871	872 879	118 (7)	180 $\left(\frac{45\pi}{64}\right)$
8 15	880 887	888 895	119 (7)	188 $\left(\frac{47\pi}{64}\right)$
8 15	896 903	904 911	120 (7)	196 $\left(\frac{49\pi}{64}\right)$
8 15	912 919	920 927	121 (7)	204 $\left(\frac{51\pi}{64}\right)$
8 15	928 935	936 943	122 (7)	212 $\left(\frac{53\pi}{64}\right)$
8 15	944 951	952 959	123 (7)	220 $\left(\frac{55\pi}{64}\right)$
8 15	960 967	968 975	124 (7)	228 $\left(\frac{57\pi}{64}\right)$
8 15	976 983	984 991	125 (7)	236 $\left(\frac{59\pi}{64}\right)$
8 15	992 999	1000 1007	126 (7)	244 $\left(\frac{61\pi}{64}\right)$
8 15	1008 1015	1016 1023	127 (7)	252 $\left(\frac{63\pi}{64}\right)$

SPREAD COUNTER	UPPER ADDRESS	LOWER ADDRESS	LEVEL (Level) COUNTER	COEFFICIENT ADDRESS
4 7	0 3	4 7	128 (8)	0
4 7	8 11	12 15	129 (8)	4 ($\pi/64$)
etc	etc	etc	etc	etc
↓	↓	↓	↓ ↓	↓
4 7	1016 1019	1020 1023	255 (8)	253 ($27\pi/128$)
2 3	0 1	1 2	256 (9)	0 (0°)
2 3	3 4	4 5	257 (9)	2 ($\pi/128$)
etc	etc	etc	etc	etc
↓	↓	↓	↓ ↓	↓
2 3	1020 1021	1022 1023	511 (9)	255 ($255\pi/256$)

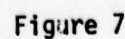
TABLE 9.SPAC DELAYS

CLOCK DRIVER (CLOCKF → CLOCKT) for LOWER ADDRESS COUNTER	10 → 30 ns
D FLIP FLOP PROPAGATION TIME (CLOCKT → FF OUT)	10 → 30 ns
LEVEL & SPREAD SENSE GENERATE (FF OUT → LEVOUTF) includes	50 → 100 ns
FF Carry In Delay	25 ns
10n generate	30 ns
Level generate	15 ns
Level Output Driver	<u>30 ns</u> 100 ns
LEVEL & SPREAD PROPAGATE (LEVINF → LEVOUTF)	30 → 60 ns
LOWER ADDRESS COUNTER CARRY PROPAGATE (CILOF → COLOF)	30 → 60 ns
UPPER ADDRESS, COEFFICIENT ADDRESS COUNTER CARRY PROPAGATE (CIUPF → COUPF) or (CICOEF → COCOEF)	20 → 100 ns
ADDRESS OUTPUT DRIVERS (FF OUT → ADDRb)	10 → 60 ns
2 ⁿ Adder Delay (CLOCKF _(SHIFT REG) → COADD) 1 stage delay only through adder	30 → 100 ns
COEF SEL to COEF ADDRESS OUTPUTS	10 → 60 ns

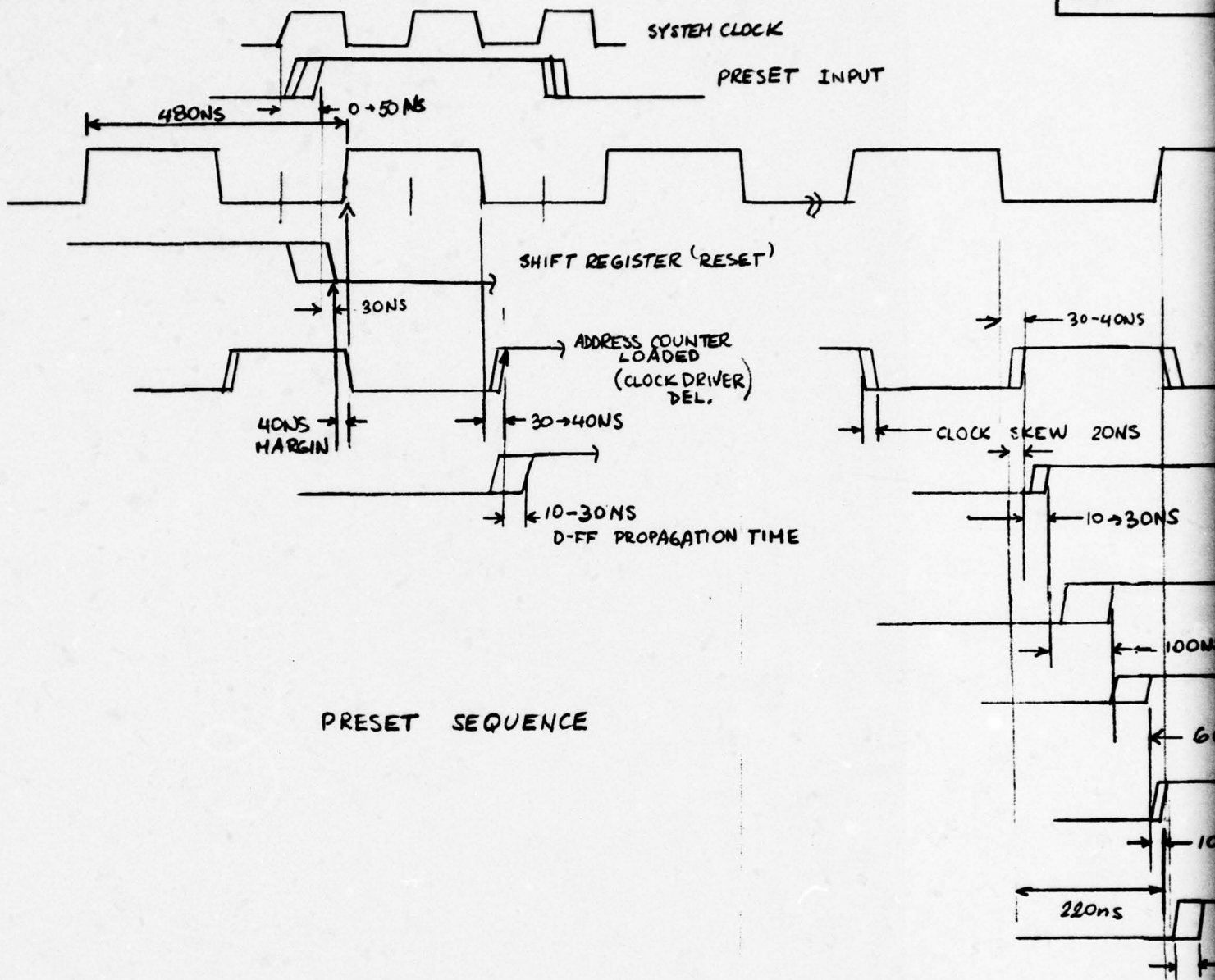
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FFT Arithmetic Butterfly



SK



PRESET SEQUENCE

LEVEL SEQUENCE

SK

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DESCRIPTION

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CLOCKF

INTERNAL 'CLOCKT'

FF PROPAGATION TIME

(CLOCKT → FF OUT)

LEVEL OR SPREAD SENSE
& GENERATE

(F/F OUT → LEVOUTF)

LEVEL OR SPREAD PROPAGATION / OR LOWER ADDRESS COUNTER
(THROUGH 1 SPAC) CARRY PROPAGATION

(LEVINF → LEVOUTF)

SHIFT REG CLOCKENABLE (TLEVINF)

SHIFT REG CLOCK DEL 10-60 NS

MARGIN = 30 NS

ENGINEERING SKETCH

ORIGINATOR

DATE

Alfred S. Hamer 10/4/75

MJO

TRW
SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SPAC
CRITICAL TIMING PATHS

SIZE

CODE IDENT NO.

B

11982

SK Figure B

SCALE

311

SHEET 1 OF

2

SK

REVISIONS

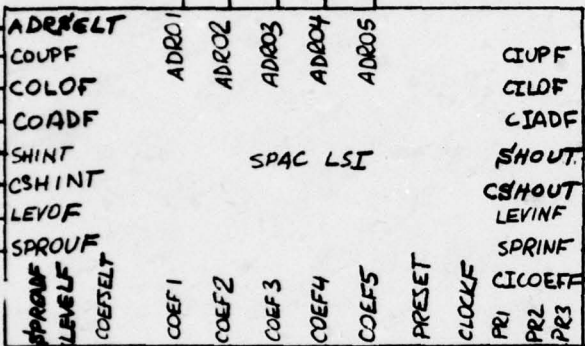
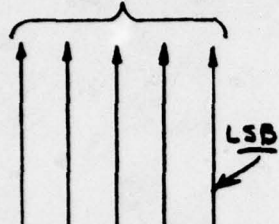
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DESCRIPTION

DATE

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LSF OF VECTOR ADDRESS



Last Level to SPAC 6
KERNEL
Microcontroller.

$\frac{\pi}{32}, \frac{\pi}{64}, \frac{\pi}{128}, \frac{\pi}{256}, \frac{\pi}{512}$

Fixed Coefficient LSF Addresses

PROGRAM
INPUT

THIS CONNECTION
USEFUL FOR
FFT ADDRESSES
FOR FFT SIZES
OF →

1024
512
256
128
64
32
16
8
4

ENGINEERING SKETCH

ORIGINATOR

Alfred S. Harmon

DATE

9/3/75

MJO

TRW

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ONE SPACE PARK • REDONDO BEACH, CALIFORNIA

SPAC INTERCONNECT

Figure 9

SIZE

B

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SCALE

313

SHEET 1 OF

SYSTEMS 3663 REV. 12-71

2

APPENDIX G

LOW POWER T^2L LSI

CONFIGURABLE GATE ARRAY

(This LSI design approach is used in SPAC 2 chip.)

The CGA is a universal logic array developed by the Microelectronics Center of TRW. The array consists of 158 TTL NAND elements with a variety of configurations available for each gate, independently. Unused elements in the array consume no power. A mask programmed signal matrix provides a flexible method for gate interconnection. A maximum of 38 pins is available for either input or output signals.

Gate Configurations

Each gate utilized is configured by selecting a function, an output type, and a power level from columns (A), (B), and (C) below (certain output features may be combined in a single gate).

(A)	(B)	(C)
GATE CONFIGURATIONS	OUTPUT TYPE	POWER OPTION
Inverter 2-Input NAND 3-Input NAND Expander	Active Pull-up Passive Pull-up Diode Exclusion Clamp Isolation Diode	Standard: Fan-out = 10 (max) Driver: Fan-out = 50 (max) or any output

CGA2 Advantages

- Direct low power T^2L compatibility - for new logic designs or as a replacement
- Fast Turnaround - Wafers are stockpiled up to the programmed mask level.
Delivery - 60 days after receipt of logic diagram.

CGA2

Operating characteristics (OVER FULL OPERATING TEMPERATURE RANGE)

PARAMETER	TEST CONDITIONS	MIN	TYPICAL	MAX	UNITS
Operating Case Temperature		-35		+100	°C
Supply Voltage, V_{CC}		4.5	5.0	5.5	V
High-level Output Voltage, V_{OH}	$V_{CC} = 4.5V, I_{OH} = \max.$	2.4	3.4		V
Low-level Output Voltage, V_{OL}	$V_{CC} = 4.5V, I_{OL} = \max$		0.35	0.5	V
High-level Input Voltage, V_{IH}		2.0			V
Low-level Input Voltage, V_{IL}				0.8	V
High-level Input Current, I_{IH} :					
Standard Gate	$V_{IH} = 2.0V$			40	μA
Driver Gate	$V_{IH} = 2.0V$			120	μA
Low-level Input Current, I_{IL} :					
Standard Gate	$V_{IL} = 0.8V$			-120	μA
Driver Gate	$V_{IL} = 0.8V$			-360	μA
High-level Output Current, I_{OH} :					
Standard Gate	$V_{CC} = 4.5V, V_{OH} = 2.4V$			-400	μA
Driver Gate	$V_{CC} = 4.5V, V_{OH} = 2.4V$			-2.2	mA
Low-level Output Current, I_{OL} :					
Standard Gate	$V_{OL} = 0.5V$			1.0	mA
Driver Gate				6.0	mA
Propagation time:					
Standard Gate, t_{PLH}	$R_L = 3.4K, C_L = 40 \text{ pf}$		45	55	ns
" " t_{PHL}	(see Figure 1)		50	65	ns
Driver Gate, t_{PLH}	$R_L = 680\Omega, C_L = 200 \text{ pf}$		35	45	ns
" " t_{PHL}	(see Figure 1)		45	60	ns
Power Consumption:					
Standard Gate ('0')			0.5	0.65	mW
" " ('1')			1.0	1.3	mW
Driver Gate ('0')			1.3	1.75	mW
" " ('1')			7.1	9.5	mW

Chip size: 205 x 205 mils

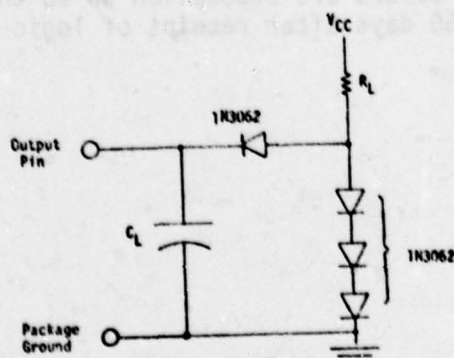
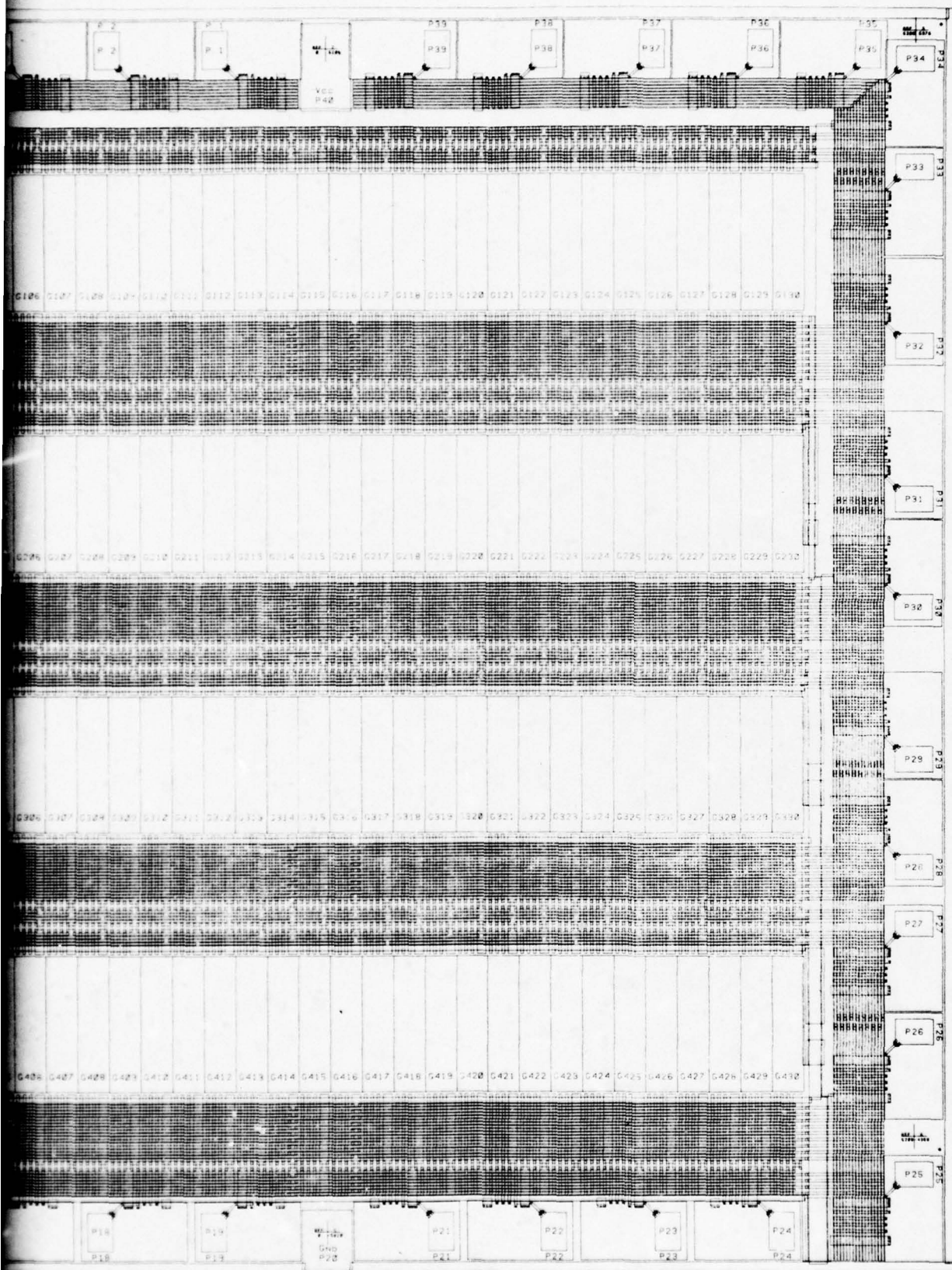
Package: 40-pin DIP or 40-pin
FLAT PACK

Figure 1. Gate Load for Propagation Delay Measurements.



2

PROGRAMMING THE CGA-2

To understand the CGA approach to logic design each part of the chip should be discussed. We will begin with the gate elements.

LOGIC GATES

On the CGA-2 worksheet (Figure 1) are 120 long rectangles labeled G101 thru G430 and 38 rectangles around the edge labeled P1 thru P38. This worksheet is actually a computer plot of some of the levels of the CGA-2 chip and the rectangles denote the locations of internal gates and pad gates, respectively.

Figures 2 and 3 show the schematic of these gates. The "X" indicates discretionary contacts that determine the function of the gate. (A straight line through an "X" is a continuous conductor. Intersecting lines are connected with a programmed contact.) The internal and pad gate circuits are identical and, though the contact arrangement varies slightly, all circuit functions can be implemented with either gate type. Possible circuit functions are:

- o standard gate, open collector, 3-input NAND
- o standard gate, active pull-up, 3-input NAND
- o three-input gate expander
- o 5K-ohm pull-up resistor
- o 25K-ohm pull-up resistor
- o isolation diode for use with pull-up resistors
- o driver gate, open collector, 3-input NAND
- o driver gate, active pull-up, 3-input NAND
- o three-diode excursion clamp

A few restrictions are placed on combining these within one gate location:

- o A gate location may contain only one gate type (standard, driver, or expander).
- o Excursion clamps are not allowed with active pull-up gates.
- o An isolation diode can be used only with a pull-up resistor.
- o Only one pull-up resistor (5K or 25K) can be used.

These restrictions place no serious limitation on the flexibility of the configurable gate.

The configuration options can be specified using a configuration code consisting of a letter and four numbers. The letter, P or I, indicates whether the contact pattern defined applies to a Pad or Internal gate. The four digits

are an octal code describing the combination of options chosen. These are determined from the CGA-2 Gate map (Figure 4) as shown. The first example is a driver gate with active pull-up and 3 inputs. The second is a driver gate expanded from the right with 3 inputs, passive pull-up, and 25K pull-up resistor with isolation diode and excursion clamp.

Once the contacts are selected on the schematic, they are readily transferred to the layout diagram (Figs. 5 and 6) which bears a 1:1 component and contact correspondence with the schematic, but the contacts are arranged physically as they are on the actual gate layout. (Figs. 7 and 8) After checking, the layout is taken to the Applicon Graphics System where a cell is created containing only the contact required. The corresponding logic symbol is drawn in the cell and a label is attached. Figure 9 shows the contents of the cell. The contacts are emphasized with a cross for clarity in plots, but only the square contacts themselves will be employed in mask generation. A final plot is run with the cell superimposed on a gate cell exactly as it will be placed in chip programming (Fig. 10). The plot is checked and filed for reference, and the cell is stored in a tape library of such cells.

When a configuration is first used, it is again checked for correctness and the circuit operation is verified when fabrication is completed. The configuration is then listed as verified with any pertinent performance specifications and can be reused in future designs with great confidence.

INTERCONNECT MATRIX

Again, looking at the worksheet (Fig. 1 is a 50% reduction of an actual worksheet), the logic gate locations just discussed are recognized and a matrix of interconnect paths is evident. It consists of diffused tunnels crossing longer metal runs. Signals may enter or leave internal gates by the top and/or bottom. All inputs are on narrow tunnels, to reduce parasitic capacitance, while outputs are through wide tunnels to reduce parasitic resistance. The inputs to the gates are labeled A, B, and C starting with the input tunnel nearest the output tunnel for that gate. Connection between a tunnel and a metal line is made by specifying a contact hole at their point of intersection. Connection may be made from a bonding pad to the output of the gate at that pad site, the "A" input of that gate, or into the matrix.

Though the layout is principally a matter of intuition and trial and error, a few general guidelines speed the process.

- **Locate Gates Driving Off-Chip First**

In an effort to maintain high off-chip drive capability, it is recommended that a gate driving off-chip be located at the site of the pad it is driving to reduce parasitic resistance between the gate and the pad.

- **Locate Gates Driven From Off-Chip Next**

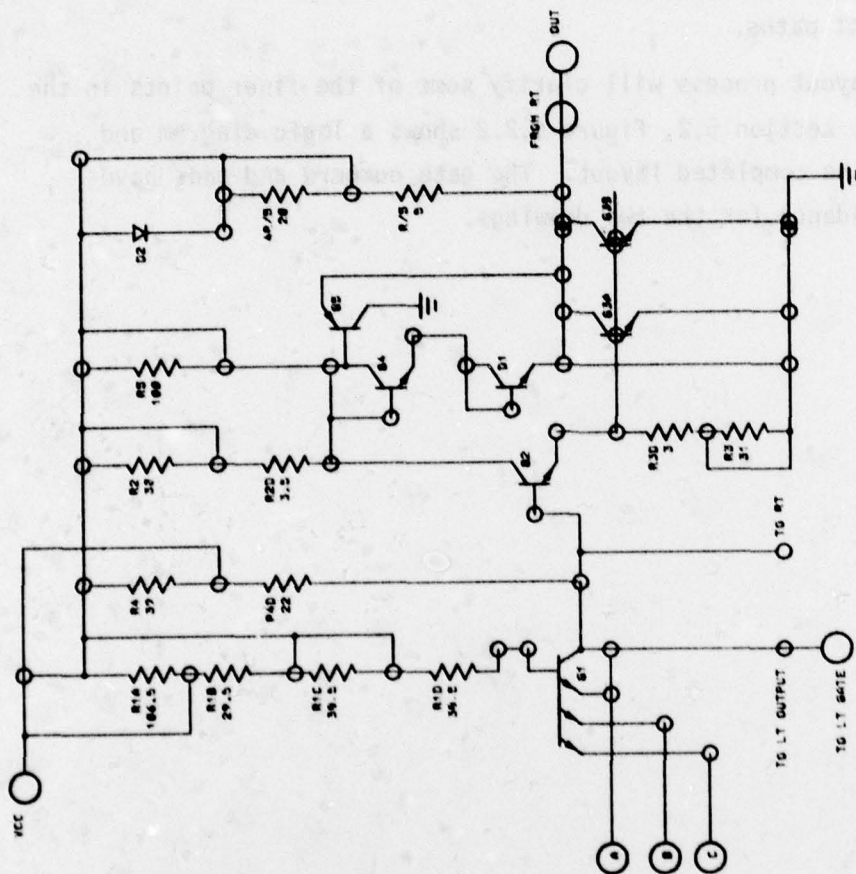
In a similar effort to reduce parasitic capacitance on inputs, try to locate an input gate next to its pad.

- **Layout For Minimum Parasitics**

Keep in mind that metal is much preferable to tunnel. In most cases, IR drop appears to be a limiting factor rather than capacitance. Table 1 gives some representative values of parasitics for the various interconnect paths.

An example of the layout process will clarify some of the finer points in the design. In the text section 5.2, Figure 5.2.2 shows a logic diagram and Figure 5.2.6 shows the completed layout. The gate numbers and pads have one to one correspondence for the two drawings.

REV. 1.1	DESCRIPTION	DATE	APPROVED



INTERNAL GATE

CGA-2
INTERNAL GATE
SCHEMATIC

Figure 2

C 11982

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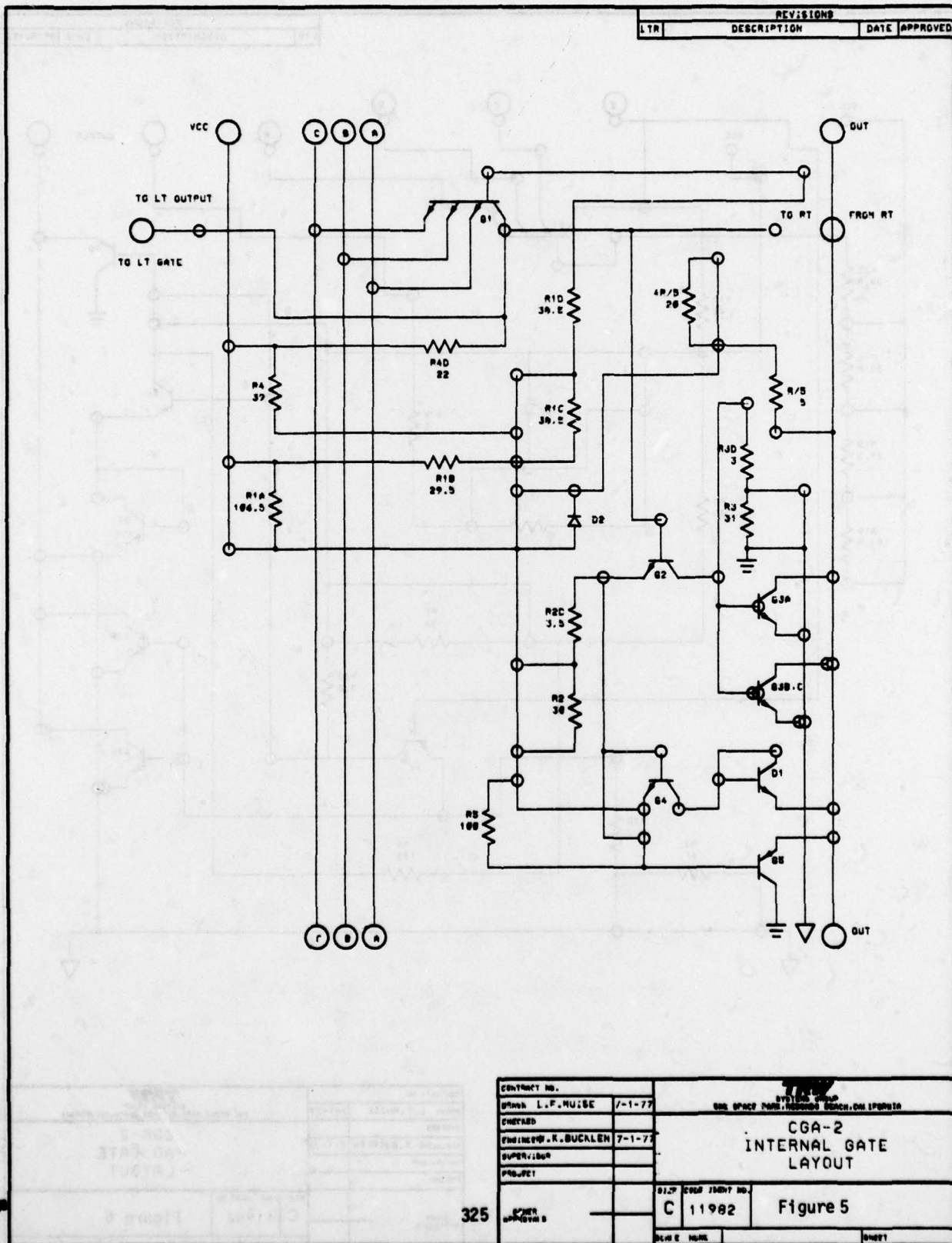
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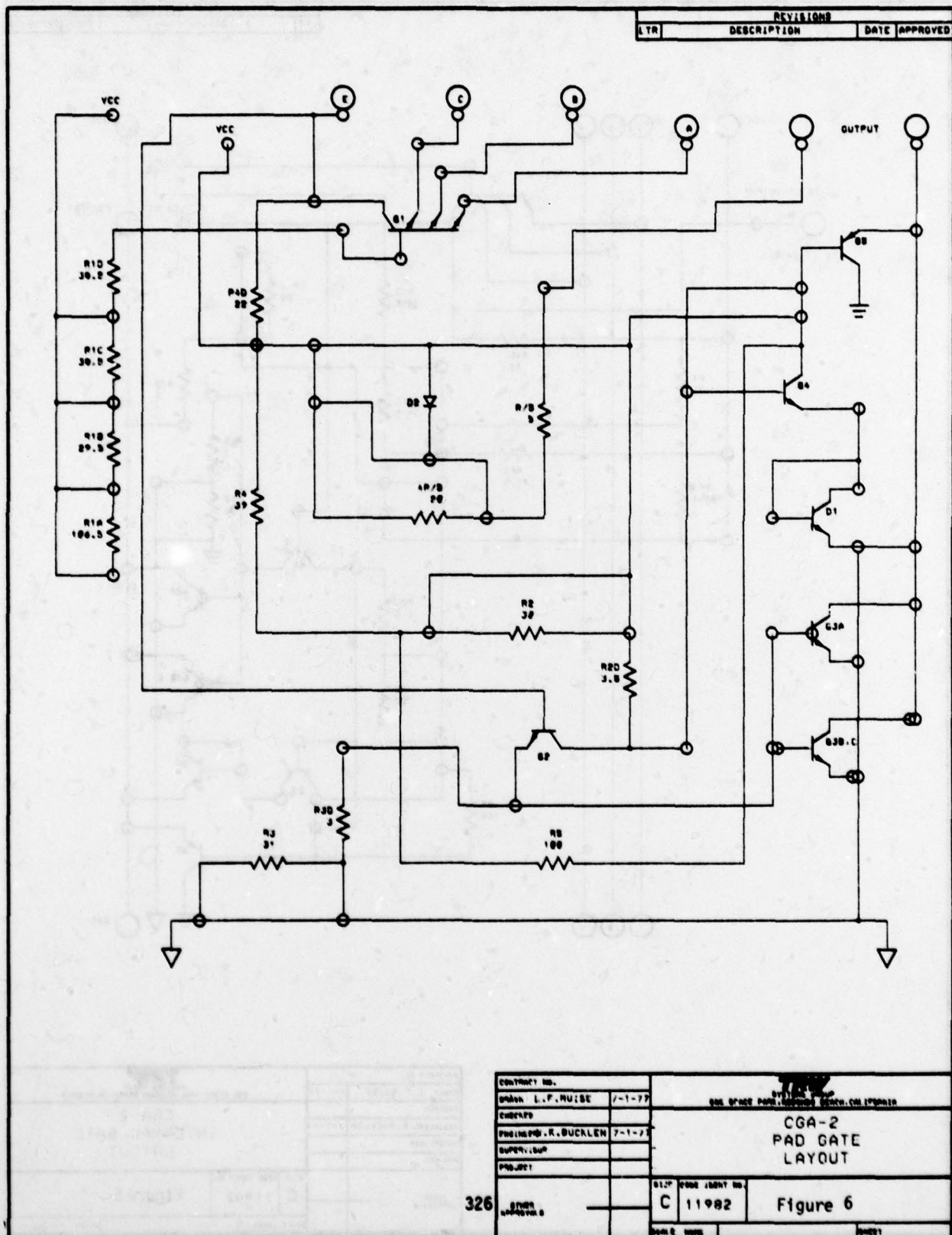
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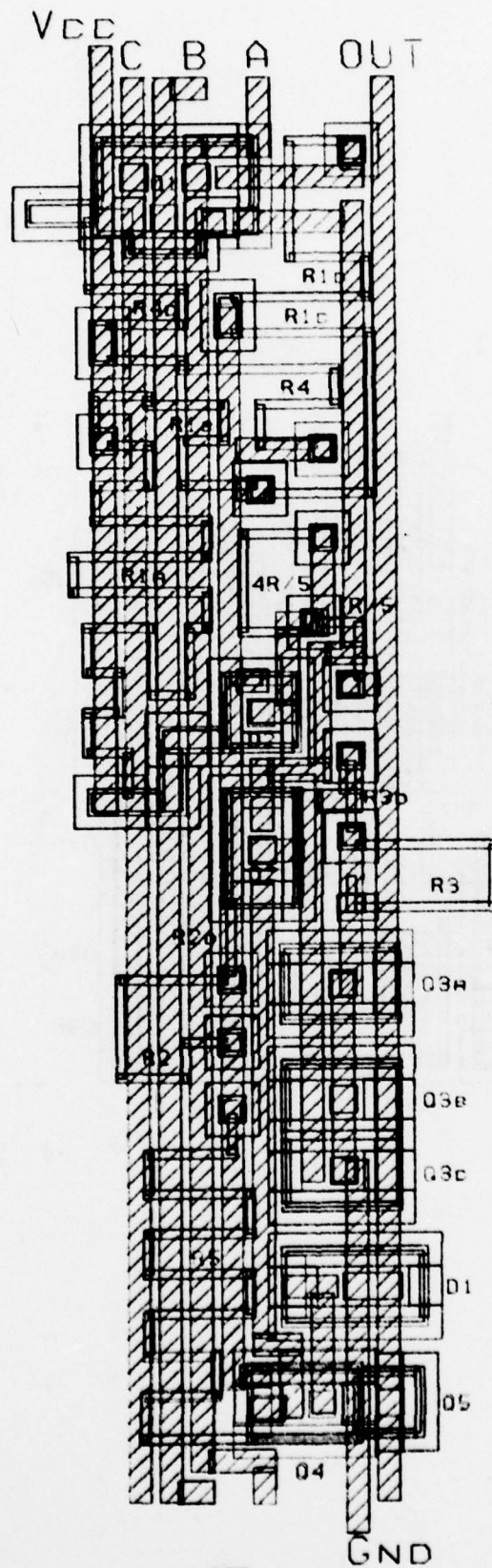


Fig. 7
Internal Gate

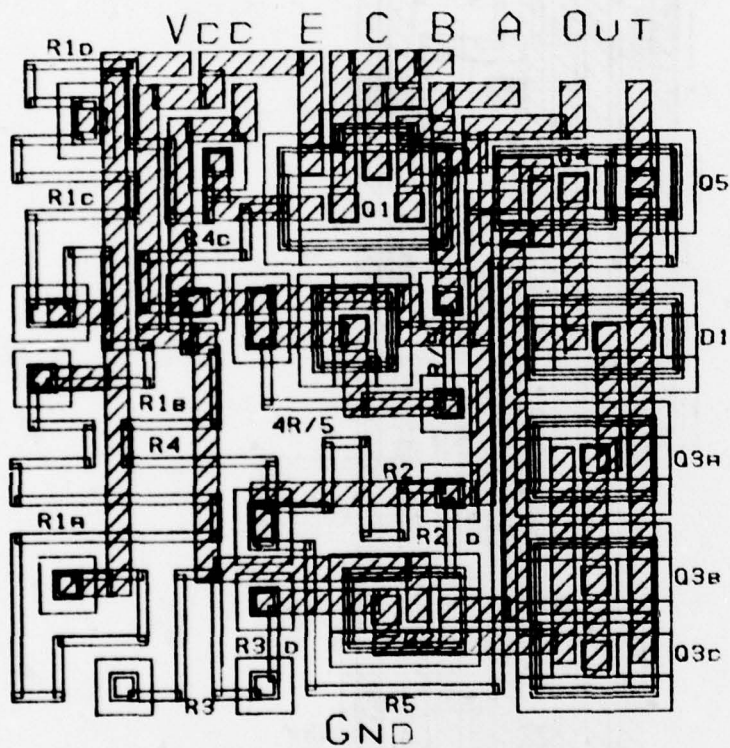
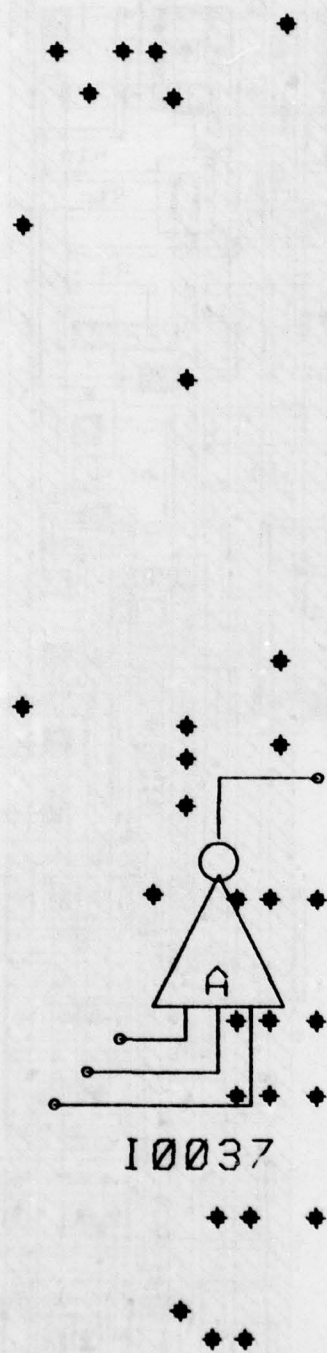
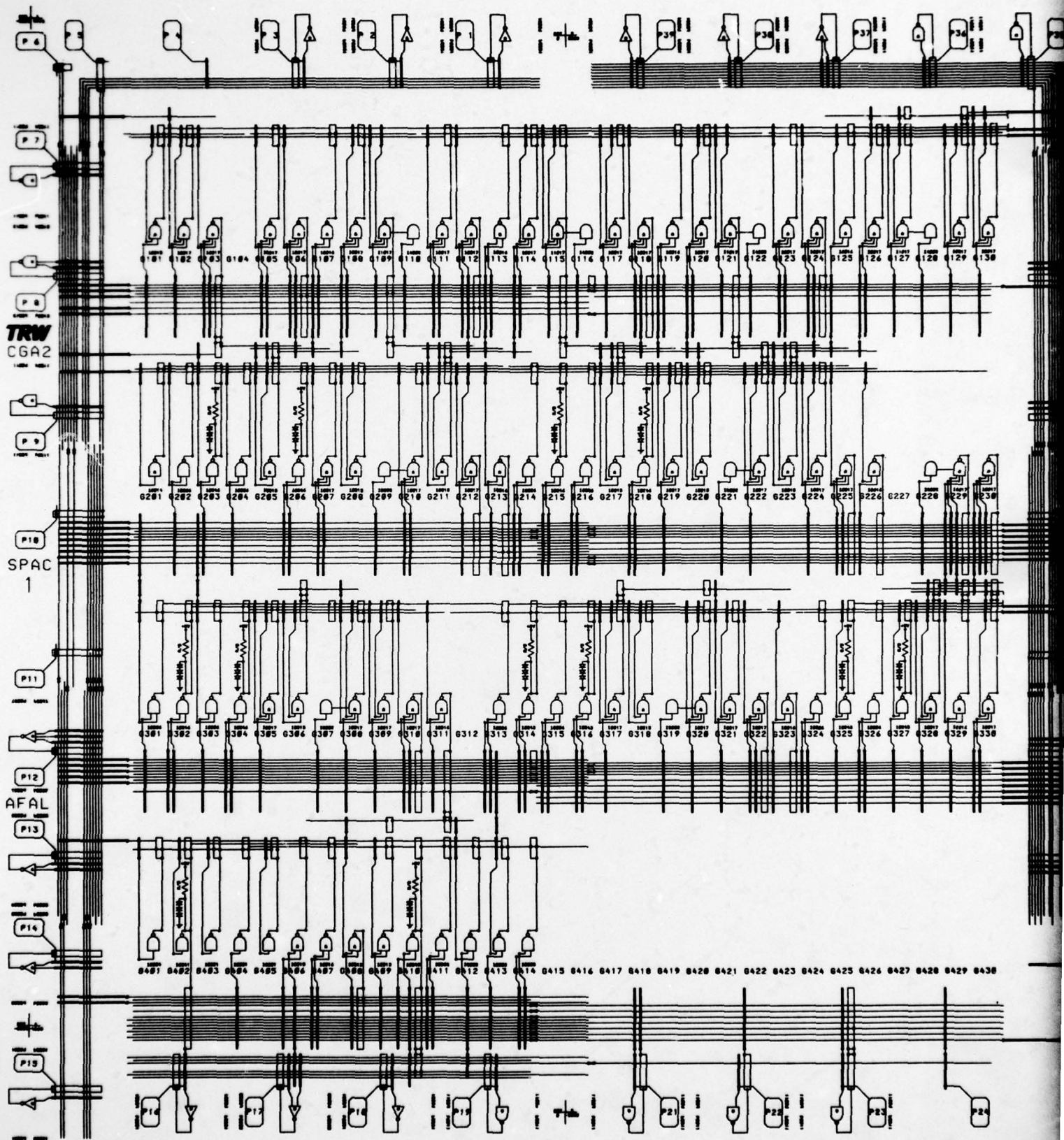


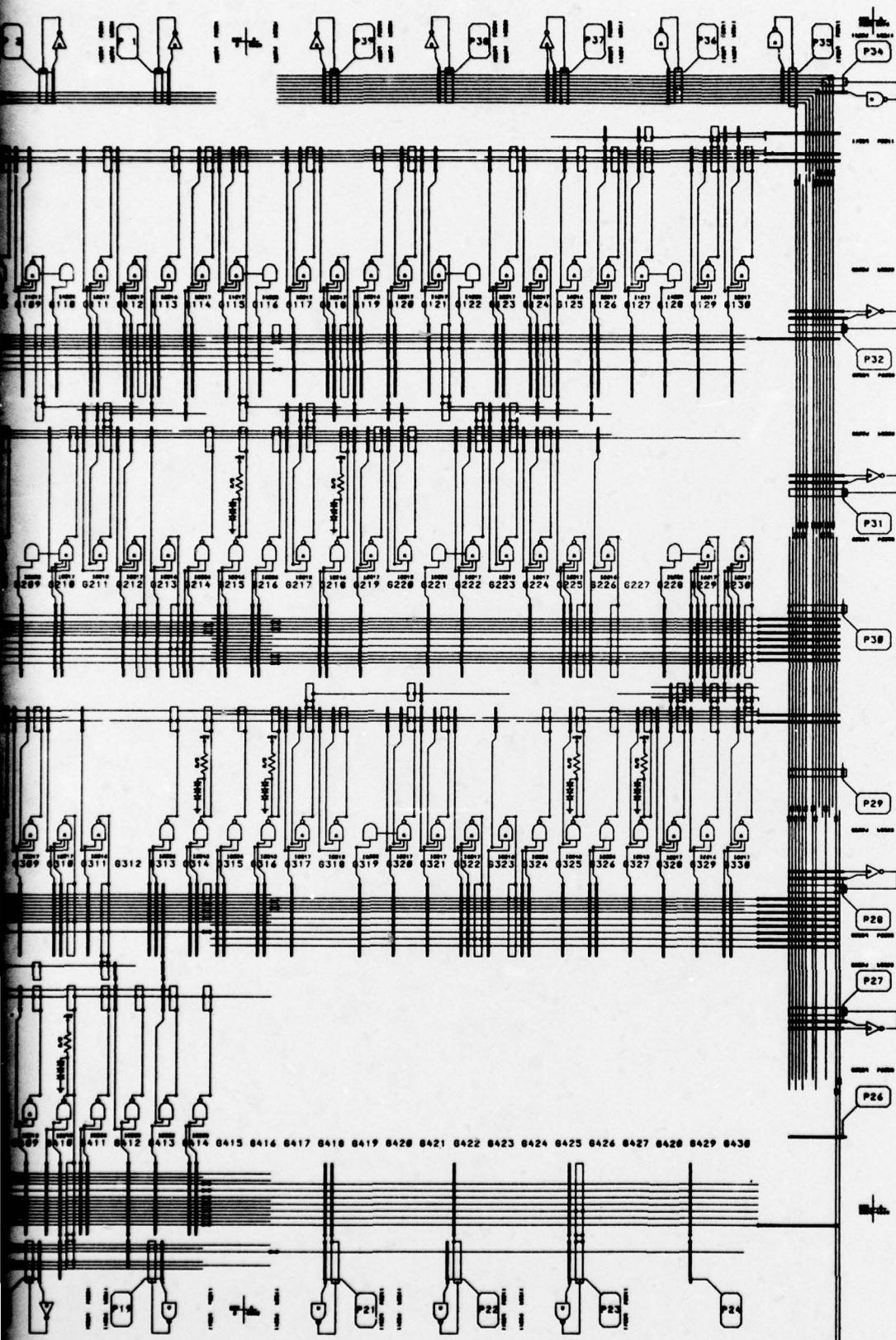
Fig. 8
Pad Gate



I0037

Fig. 9
Internal Gate
Configuration





CALCULATED INTERCONNECT PARASITICS

<u>METAL</u>		
	<u>CAP (pF)</u>	<u>RES (Ω)</u>
1 cm	4.0	29.0
1 line width	0.00056	0.00406
1 gate width	0.0056	0.0406
SHORT BUS TOP OF GATE (3 Gates)	0.017	0.122
LONG BUS TOP OF GATE (6 Gates)	0.034	0.244
SHORT BUS BOTTOM OF GATE (14 Gates)	0.784	5.684
LONG BUS BOTTOM OF GATE (16 Gates)	0.896	6.496
PAD BUS TOP	1.064	7.714
PAD BUS TOP OF SIDE	0.560	4.060
PAD BUS CENTER OF SIDE	0.448	3.248
PAD BUS BOTTOM OF SIDE	0.392	2.842
JUMPER	0.0168	0.122
INTERNAL GATE LENGTH	0.252	1.830
	<u>CAP (pF)</u>	<u>TUNNEL RES (Ω)</u>
1 line width (slim)	0.05	8.0
1 line width (wide)	0.13	2.5
TOP OF GATE (SHORT)(SLIM)	0.30	48.0
TOP OF GATE (SHORT)(WIDE)	0.79	15.0
TOP OF GATE (LONG)(SLIM)	0.40	64.0
TOP OF GATE (LONG)(WIDE)	1.05	20.0
BOTTOM OF GATE (SLIM)	1.10	175.0
BOTTOM OF GATE (WIDE)	2.88	55.0
TOP PAD GATE (SLIM)	0.55	88.0
TOP PAD GATE (WIDE)	1.44	27.5
SIDE PAD GATE (SLIM)	0.90	144.0
SIDE PAD GATE (WIDE)	2.36	45.0
BOTTOM PAD GATE (SLIM)	0.60	96.0
BOTTOM PAD GATE (WIDE)	1.57	30.0
UNDER POWER BUS (SLIM)	1.15	184.0
UNDER POWER BUS (WIDE)	3.00	57.5
JUMPER (2 METAL WIDTHS)	0.10	16.0
JUMPER (3 METAL WIDTHS)	0.15	24.0

TABLE 1